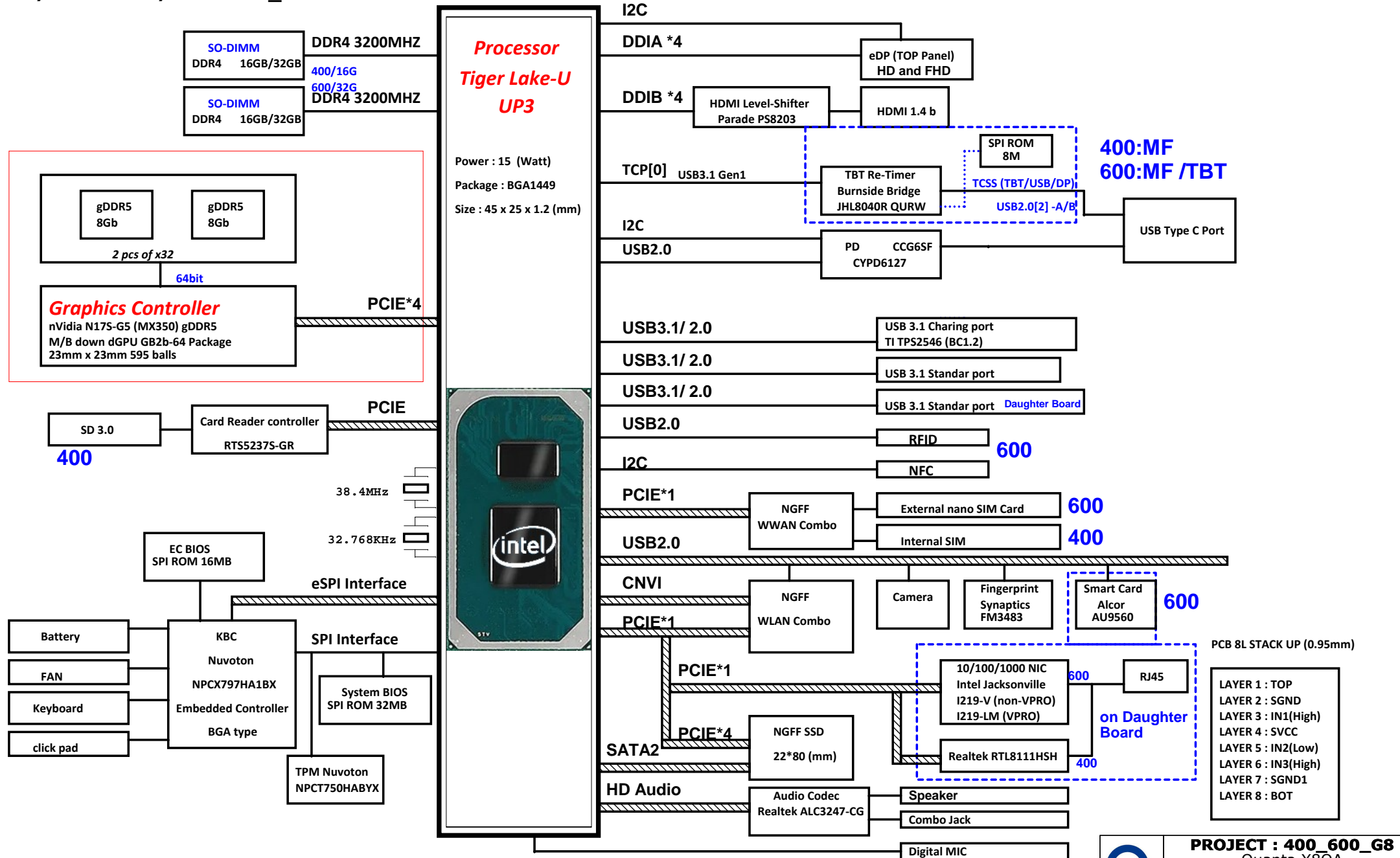
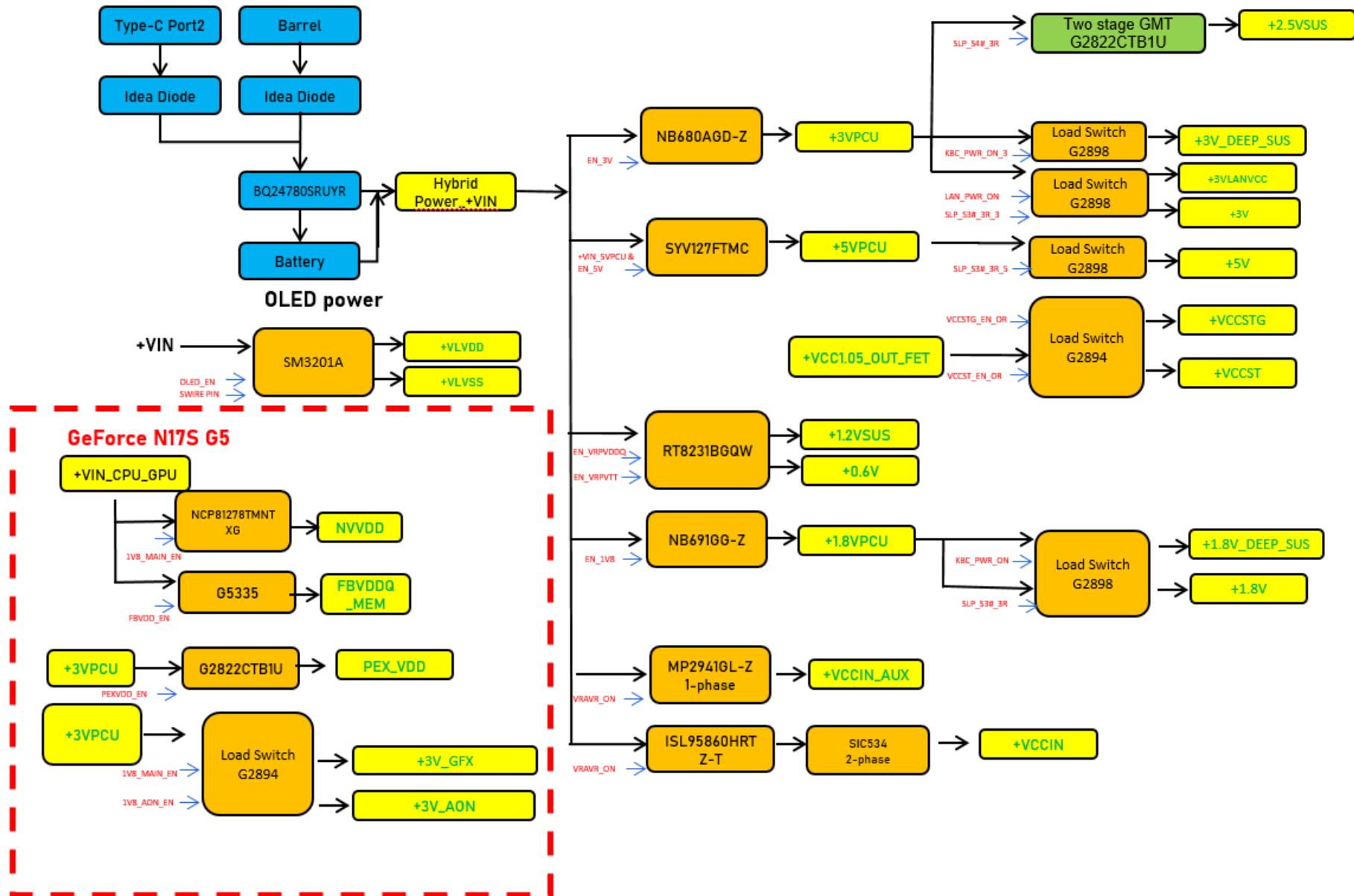
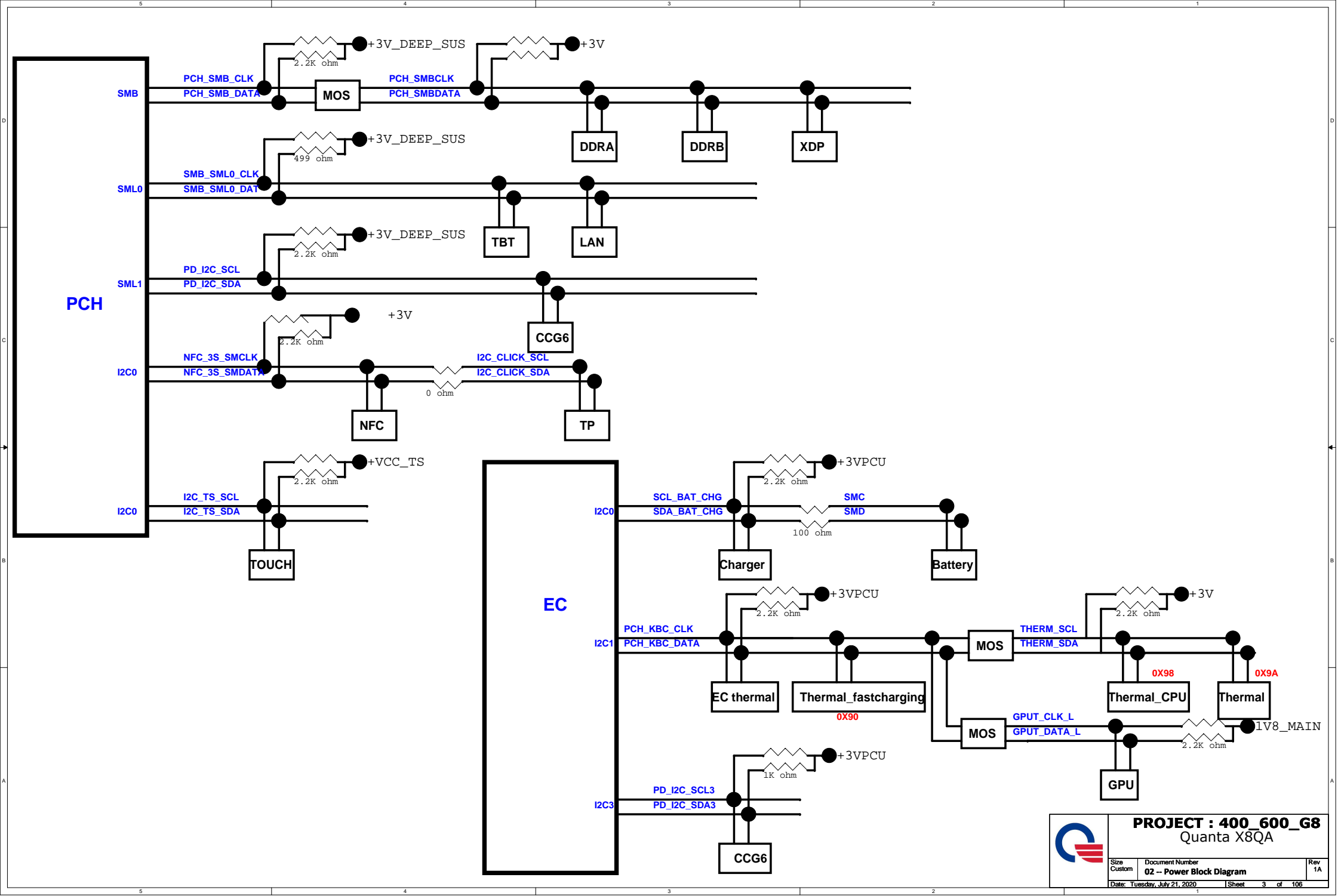


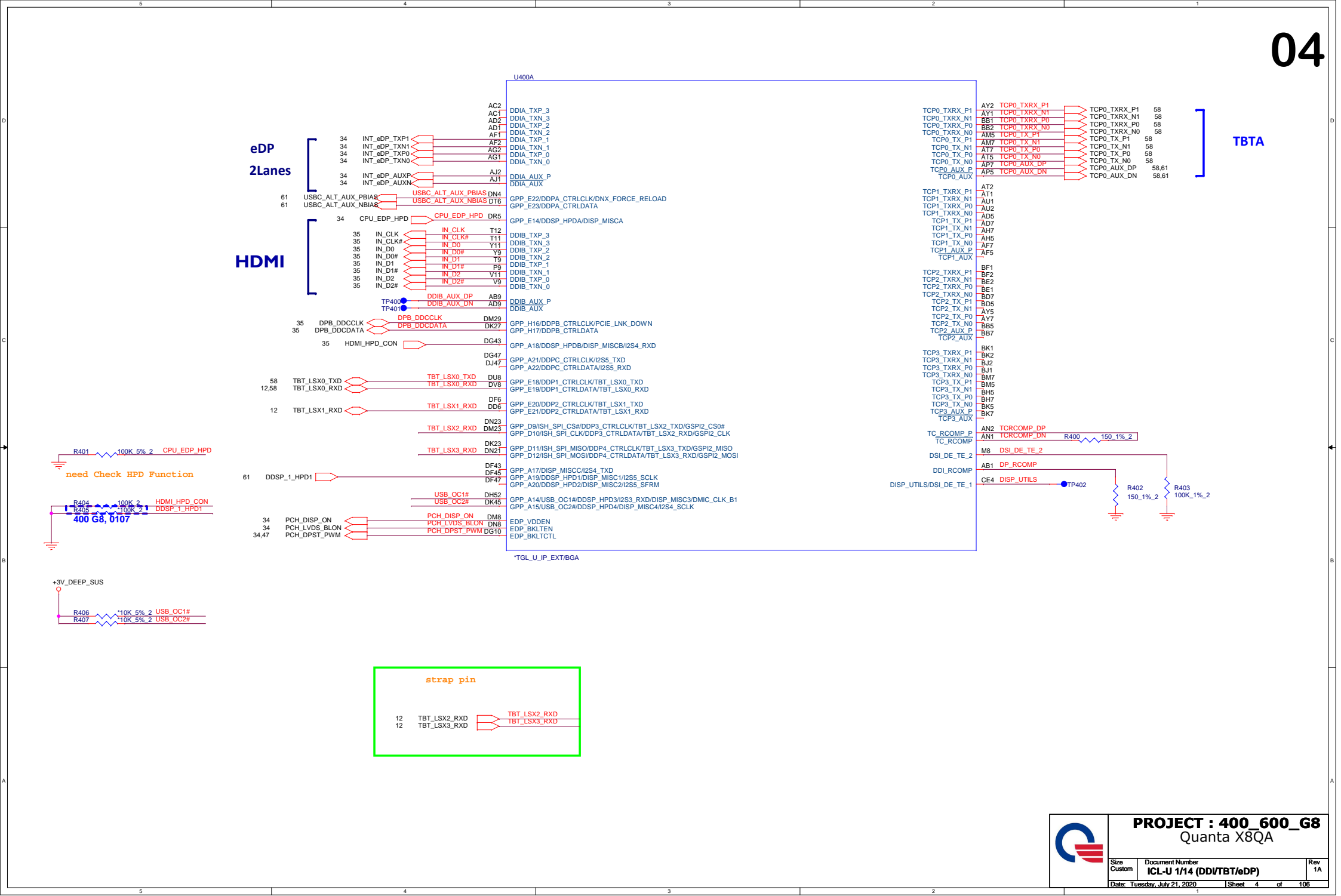
400/600 14"/15" G8_TGL

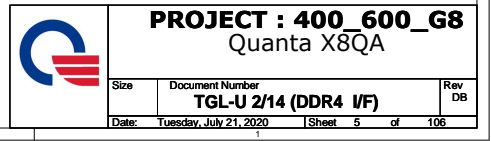


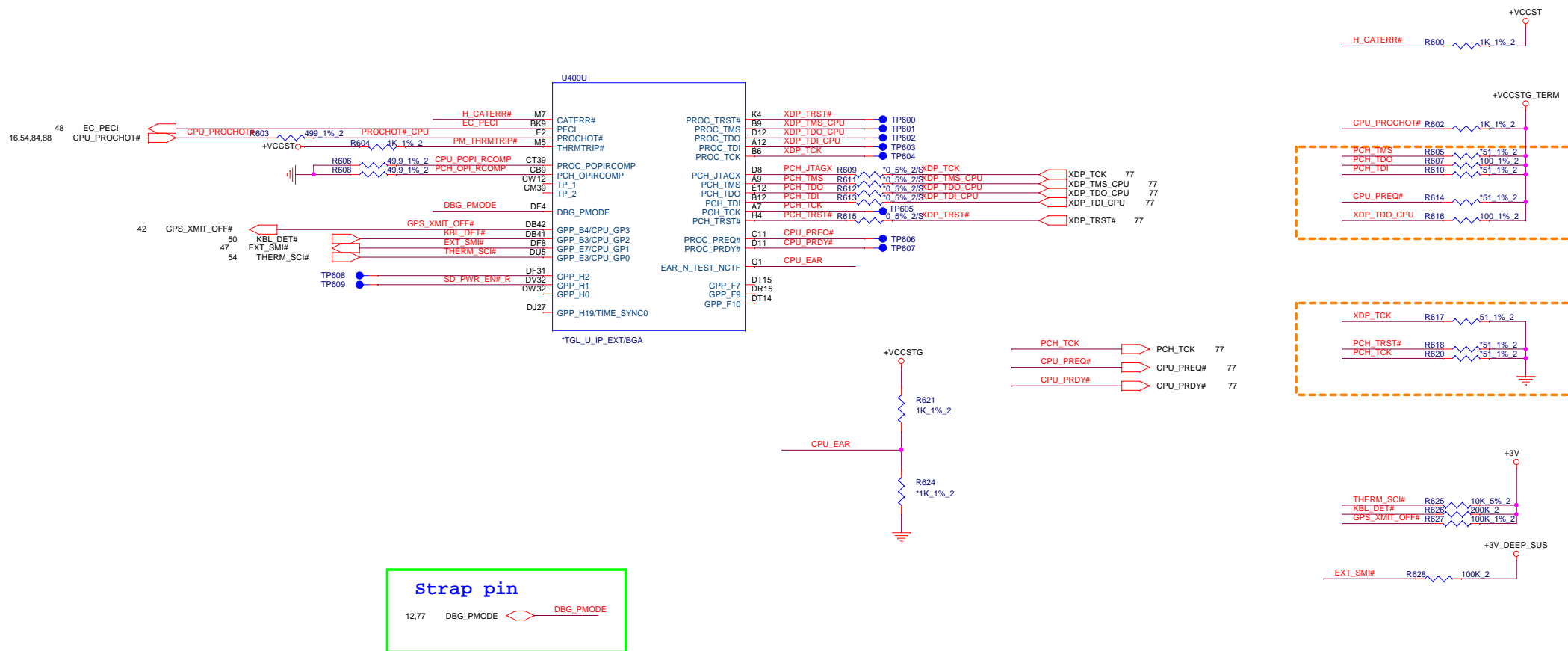
TGL-U POWER BLOCK DIAGRAM



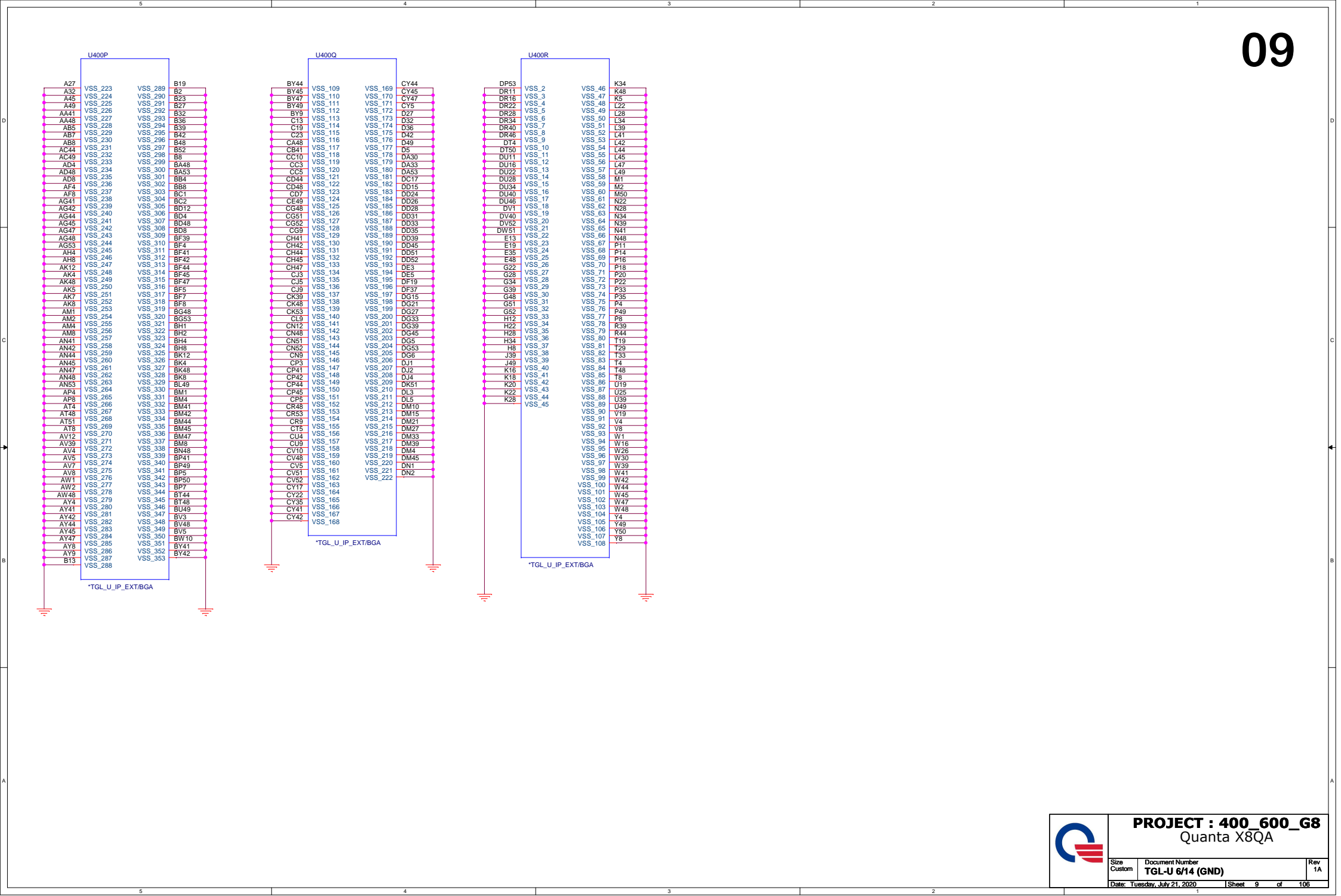


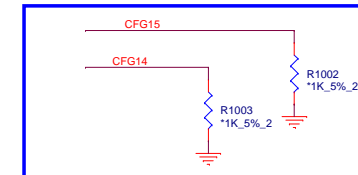
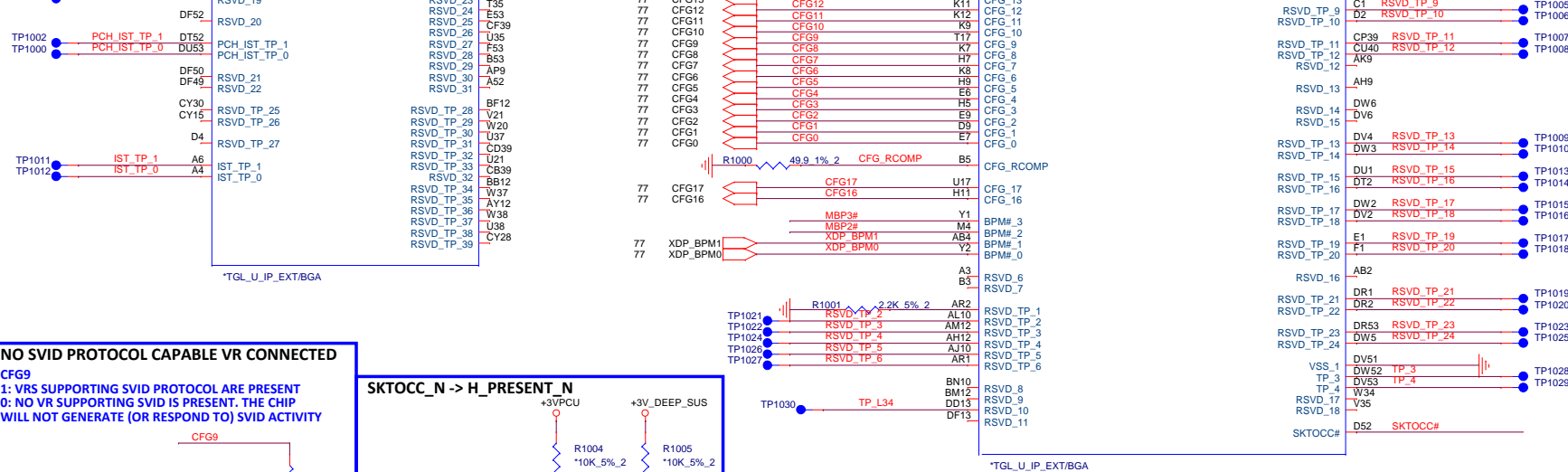












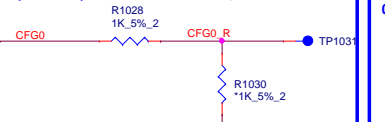
CFG9
1: VRS SUPPORTING SVID PROTOCOL ARE PRESENT
0: NO VR SUPPORTING SVID IS PRESENT. THE CHIP
WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY



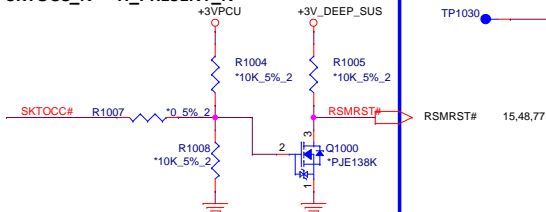
CFG10
1: POWER FEATURES ACTIVATED DURING RESETT
0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT
ACTIVATED



CFG0	1: (DEFAULT) NORMAL OPERATION; NO STALL
------	---

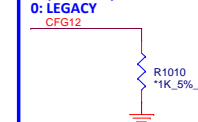


CFG1
1: (DEFAULT) NORMAL OPERATION
0: PCH-LESS MODE

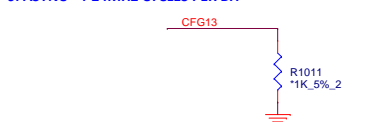


CFG12

1: (DEFAULT) PMSYNC 2.0



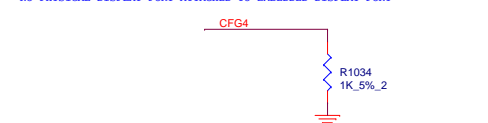
CFG13
1: (DEFAULT)SYNCHRONOUS (1 24 MHZ CYCLE PER BIT)
0: ASYNC - 4-24MHZ CYCLES PER BIT



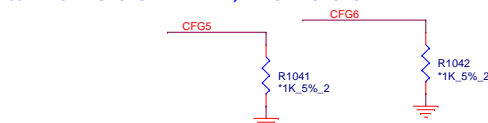
```

CFG4
1: DISABLED
    AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT
0: ENABLED
    NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

```



```
CFG[6:5]
11: DEVICE1 FUNTION 1, DEVICE 1 FUNCTION2 DISABLED
10: DEVICE1 FUNCTION1 ENABLED DEVICE1 FUNCTION 2 DISABLED
01: DEVICE 1 FUNCTION 1 DISABLED, DEVICE 1 FUNCTION 2 ENABLED
00 DEVICE 1 FUNCTION 1 ENABLED, DEVICE 1 FUNCTION 2 ENABLED
```



CFG11
1:(DEFAULT)DMI WILL BE CONFIGURED AS HALF SWING DC COUPLED
0: DMI WILL BE CONFIGURED AS FULL SWING AC COUPLED

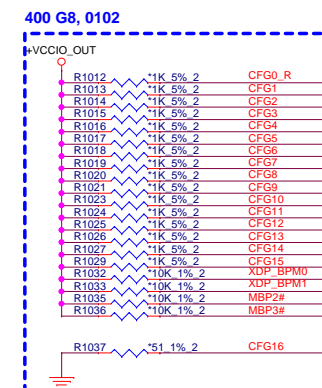
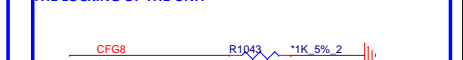


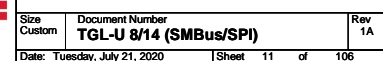
1: (DEFAULT) PEG TRAIN IMMEDIATELY FOLLOWING XXRESETB DEASSERTION
0: PEG WAIT FOR BIOS FOR TRAINING



CFG8
1: DISABLE(DEFAULT): IN THIS CASE, NOA WILL BE
DISABLE IN LOCKED UNITS AND ENABLE IN UN-LOCKED UNITS

0: ENABLED: NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT

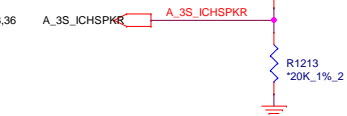




TOP SWAP OVERRIDE

High: TOP SWAP ENABLED
Low: DISABLED
WEAK INTERNAL PD 20K

GPP_B14/SPKR

**NO REBOOT**

High: NO REBOOT
Low: REBOOT ENABLED
WEAK INTERNAL PD 20K

GPP_B18/GSPI0_MOSI

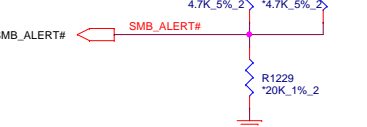


01/15 PD 10K at PAGE.8

TLS CONFIDENTIALITY

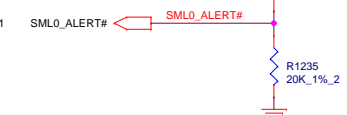
High - TLS CONFIDENTIALITY ENABLE
Low - TLS CONFIDENTIALITY DISABLE
WEAK INTERNAL PD 20K

GPP_C2/SMBALERT#

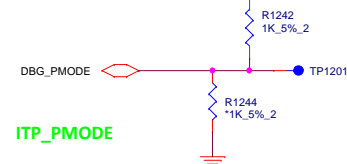
**ESPI OR EC LESS**

High: ESPI IS DISABLED
Low: ESPI SELECTED
WEAK INTERNAL PD 20K

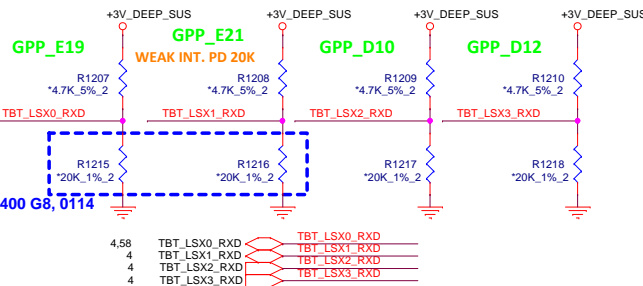
GPP_C5/SML0ALERT#

**(RSVD) ITP PMODE**

High: DFXTESTMODE DISABLED(DEFAULT)
Low: DFXTESTMODE ENABLED
WEAK INTERNAL PU 20K

**TBT LSX PINS VCCIO CONFIGURATION**

High: 3.3V
Low: 1.8V
NO INTERNAL PU/PD

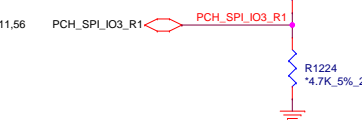
**(RSVD) XTAL INPUT MODE**

High: XTAL INPUT IS SINGLE ENDED
Low: XTAL IS ATTACHED
WEAK INTERNAL PD 20K

(RSVD) A0 PERSONALITY STRAP

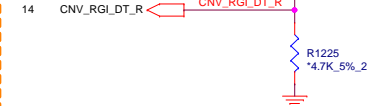
High: DISABLE
Low: ENABLE
External pull-up is required.

SPIO_IO3

**M.2 CNVi Mode Select**

High: Integrated CNVi disabled
Low: Integrated CNVi enabled
An external pull-up or pull-down is required

GPP_F2

**RING OSCILLATOR BYPASS**

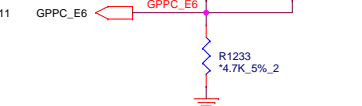
High: BYPASS MODE ENABLED
Low: RING OSCILLATOR (QUALIFIED BY DFXTESTMODE)
NO INTERNAL PU/PD

GPP_H3

**(RSVD) JTAG ODT DISABLE**

High: JTAG ODT Enable
Low: JTAG ODT Disable
External pull-up is required.

GPP_E6

**Flash Descriptor Security Override**

High: DISABLE
Low: ENABLE
WEAK INTERNAL PD 20K

GPP_R2

**CPUNSSC CLOCK FREQ**

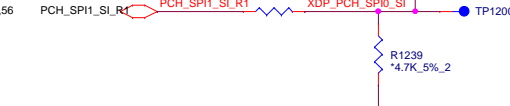
High: 19.2MHz CLOCK FROM INTERNAL DIVIDER
Low: 38.4MHz CLOCK FROM DIRECT CRYSTAL (Default)
WEAK INTERNAL PD 20K

GPP_B23/SML1ALERT#

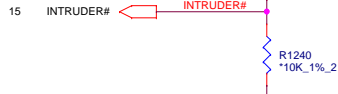
**(RSVD) BOOT HALT**

High: DISABLE
Low: ENABLE
External pull-up is required.

SPIO_MOSI



INTRUDER#

**(RSVD) CONSENT STRAP**

High: DISABLE
Low: ENABLE
External pull-up is required.

SPIO_IO2

**3V SELECT STRAP**

0 = SPI voltage is 3.3V (4.7K ohm pull-down to GND)
1 = SPI voltage is 1.8V (4.7K ohm pull-up to DSW_PWROK)



HVM ONLY

GPP_E11

XTAL FREQUENCY SEL

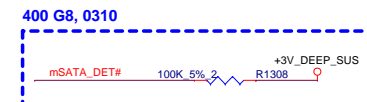
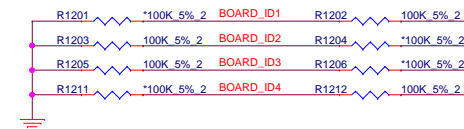
High: 24MHZ
(25 MHZ WHEN XTAL FREQ DIVIDER NON ZERO)
Low: 38.4MHZ (DEFAULT)
WEAK INTERNAL PD 20K

CNV_BRI_DT_R



PROJECT : 400_600_G8
Quanta X8QA





	BOARD ID1	BOARD ID2	BOARD ID3	BOARD ID4
DB0	0	0	0	0
DB1	0	0	0	1
DB2	0	0	1	0
	0	0	1	1
SI1	0	1	0	0
SI1B	0	1	0	1
SI2	0	1	1	0
	0	1	1	1
SI3	1	0	0	0
PV	1	0	0	1
PVR	1	0	1	0
	1	0	1	1
MV	1	1	0	0

*TGL_U_IP_EXT/BGA



PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	Type-A	Port0	USB3
Port2	Type-A	Port1	USB3
Port3	WLAN	Port2	PCI-E
Port4	Type-A	Port3	USB3
Port5	WWAN	Port4	PCI-E
Port6	NA	Port5	Un-used
Port7	SD		
Port8	LAN		
Port9	PCI-E-SSD		
Port10	PCI-E-SSD		
Port11	PCI-E-SSD		
Port12	PCI-E-SSD		

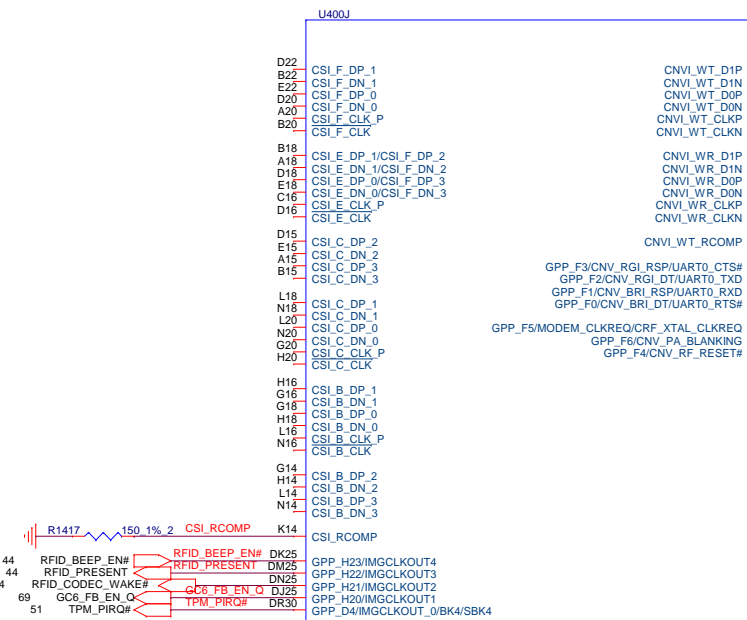
USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	USB
PORT-2	Camera
PORT-3	WWAN
PORT-4	USB
PORT-5	USB
PORT-6	Type C
PORT-7	Finger Print
PORT-8	Smart Card
PORT-9	RFID
PORT-10	BT

PCIe (Gen4)	
(Gen4)	Function
PORT-1	GPU
PORT-2	GPU
PORT-3	GPU
PORT-4	GPU



PROJECT : 400_600_G8
Quanta X8QA



Cardreader

WLAN

dGPU

LAN

WWAN

SSD

U400K

BW1

BW2

CB2

CB1

CB1

BW4

BW5

CL7

CL8

CB4

CB5

BY4

BY3

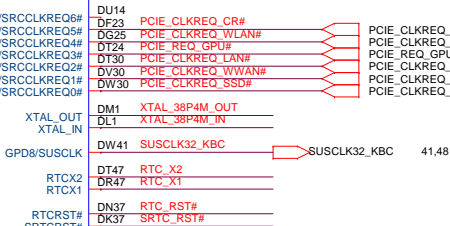
CN7

CN8

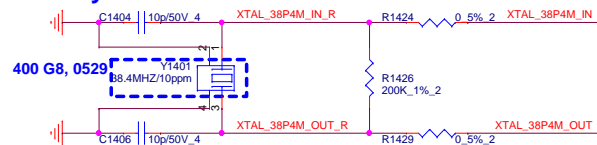
DJ5

XCLK_BIASREF

*TGL_U_IP_EXT/BGA



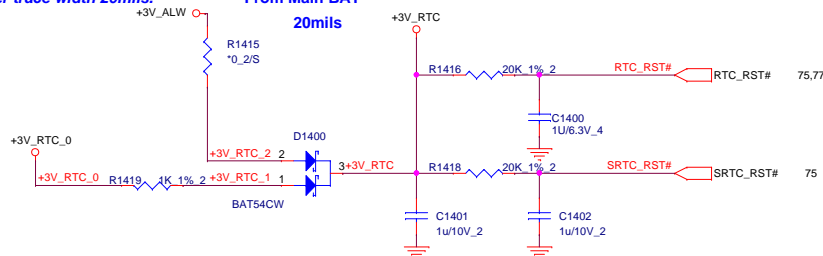
Crystal 38.4MHz

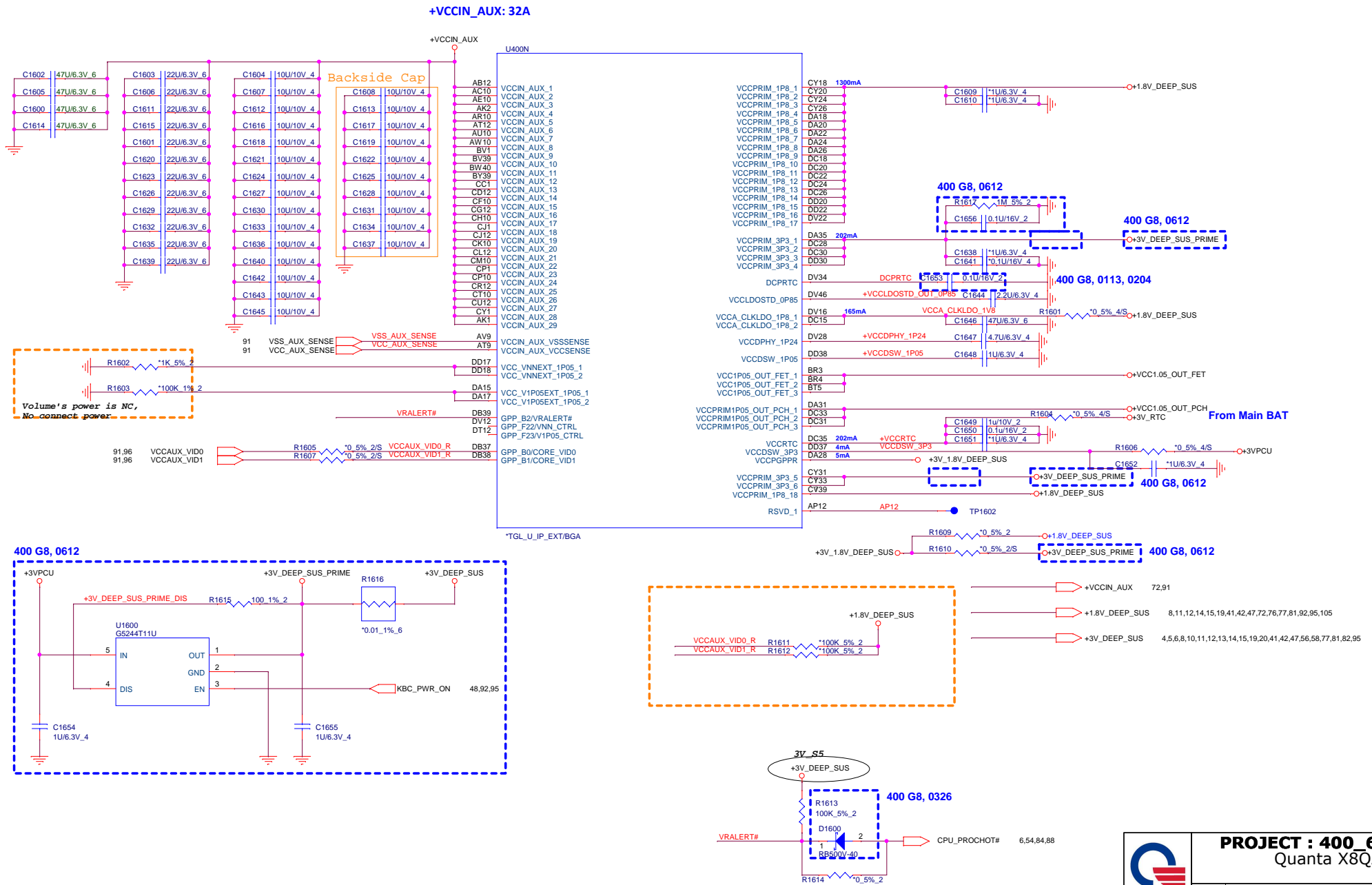


RTC Circuitry(RTC)

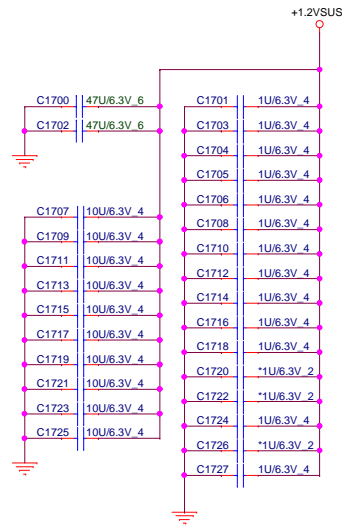
RTC Power trace width 20mils.

From Main BAT

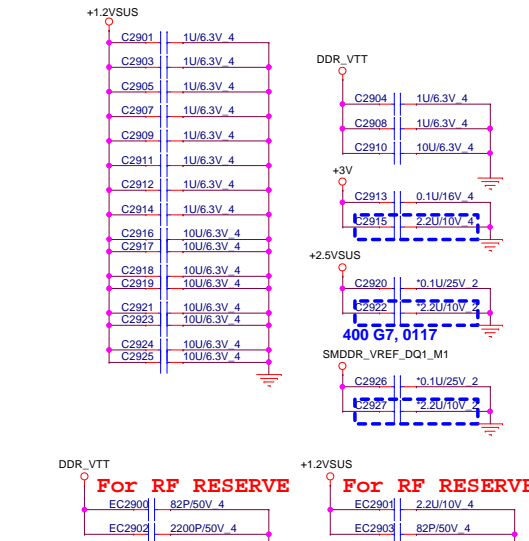




For page rule move the caps from page7 to page 17

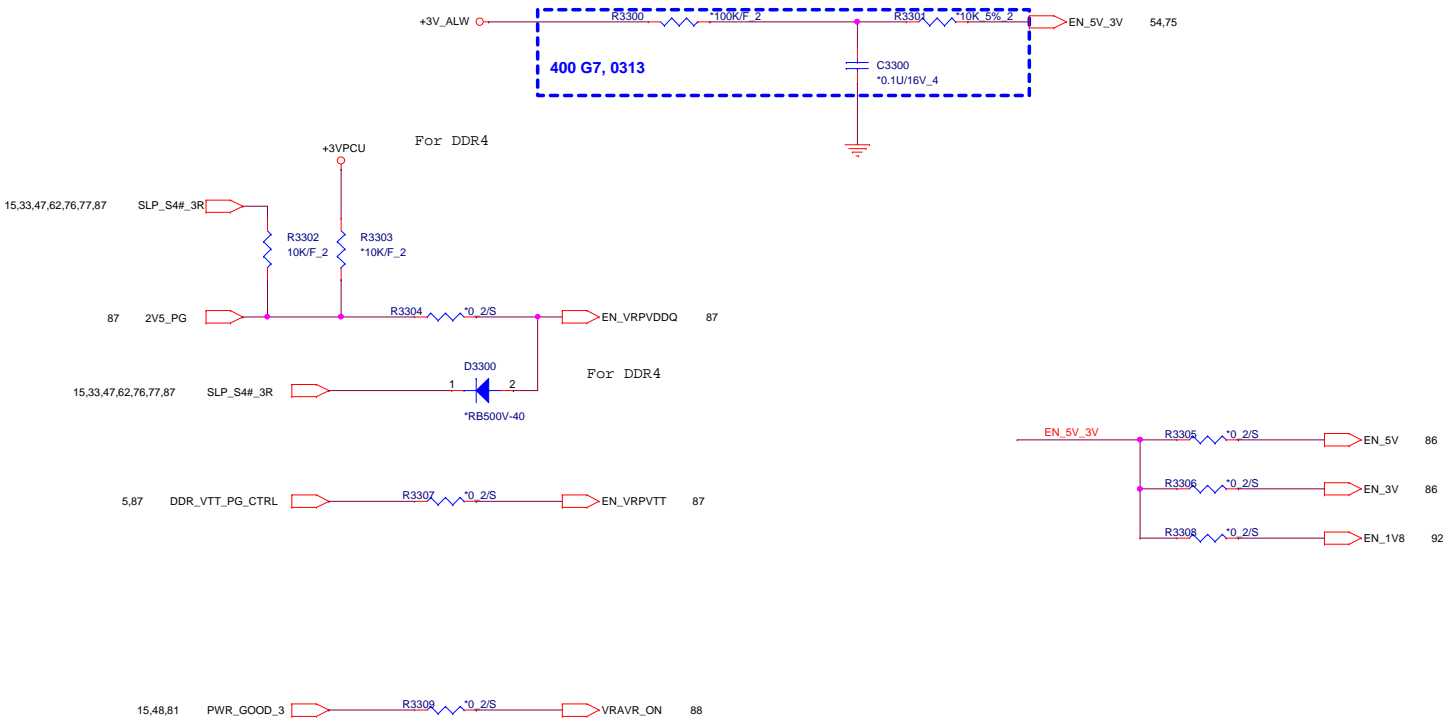




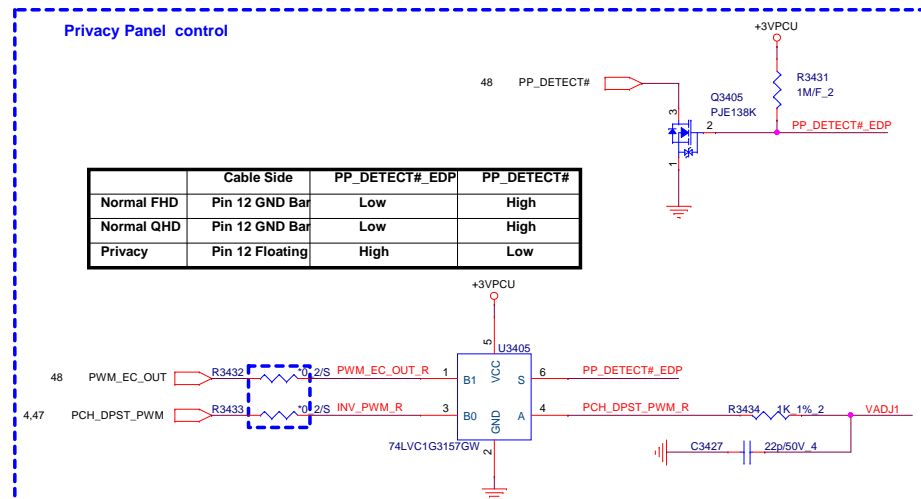
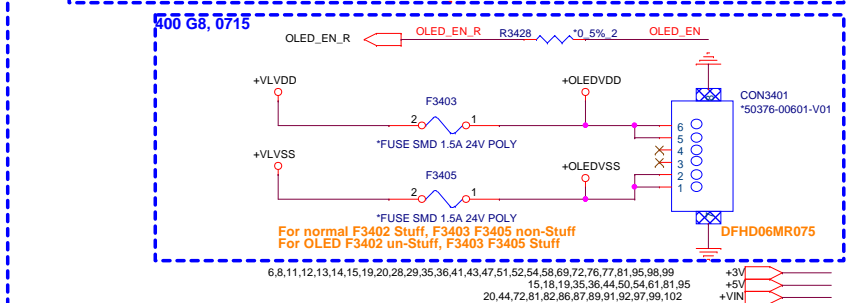
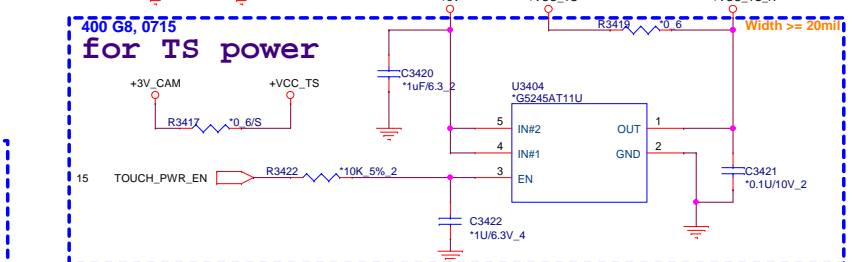
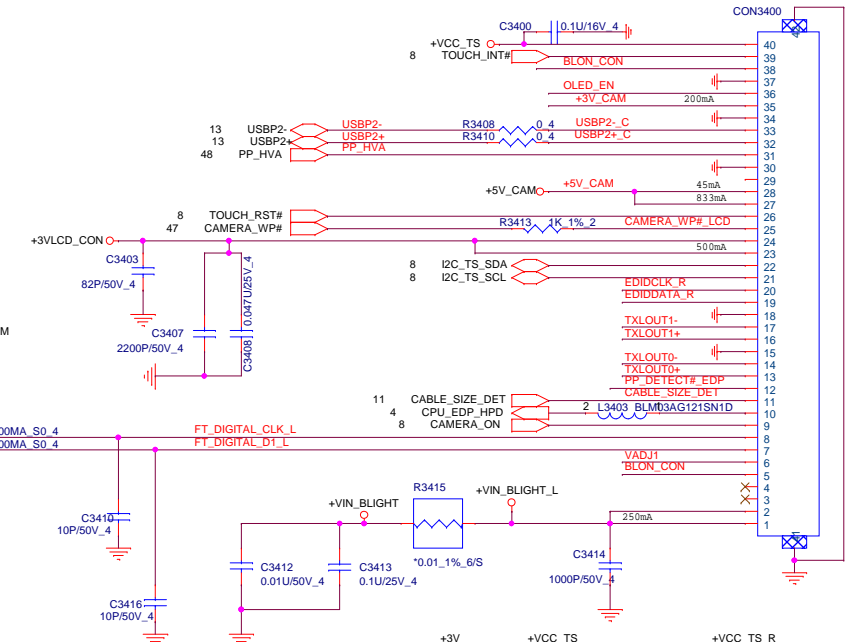
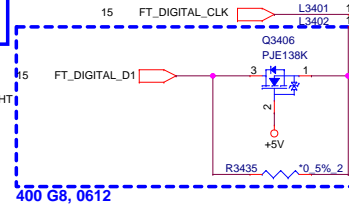
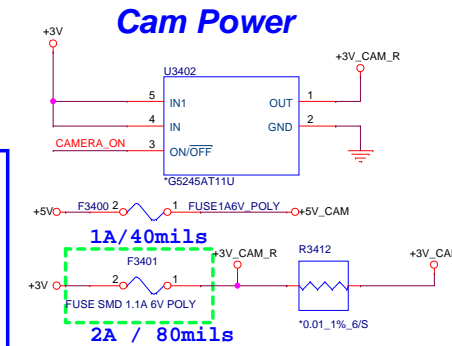
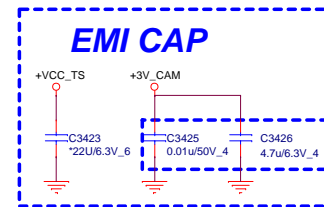
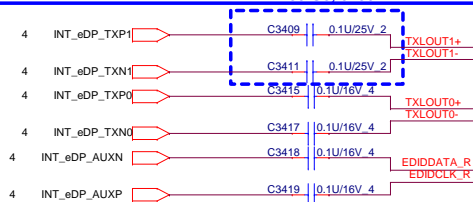
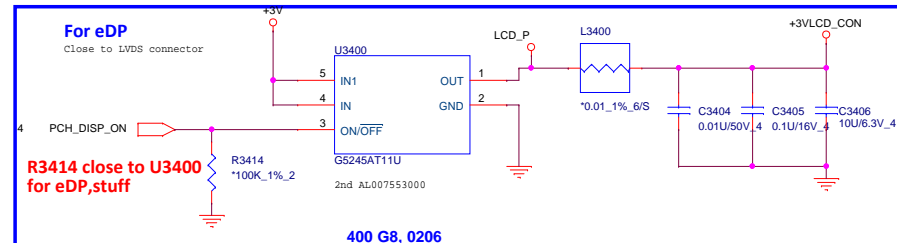
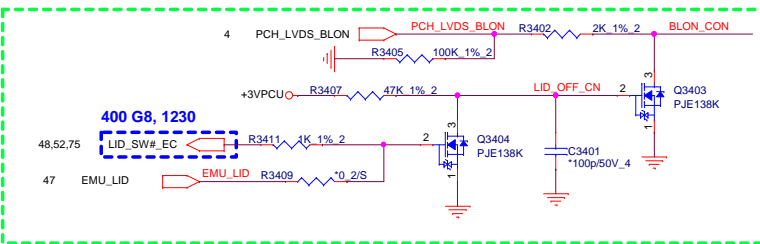


PROJECT : 400_600_G8
Quanta X8QA

400 series 1001
POWER TO EE NET NAME CONNECTION



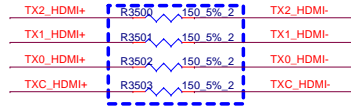
LID Switch



	Cable Side	PP_DETECT#_EDP	PP_DETECT#
Normal FHD	Pin 12 GND Bar	Low	High
Normal QHD	Pin 12 GND Bar	Low	High
Privacy	Pin 12 Floating	High	Low

400 G8, 0331

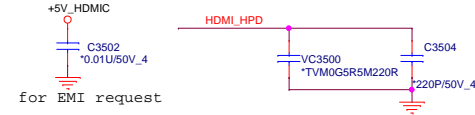
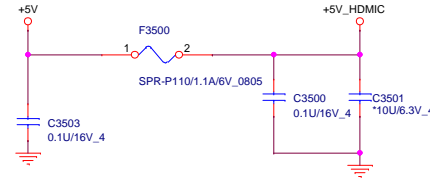
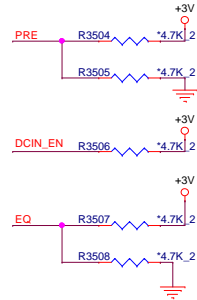
EMI Solution



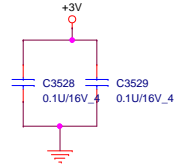
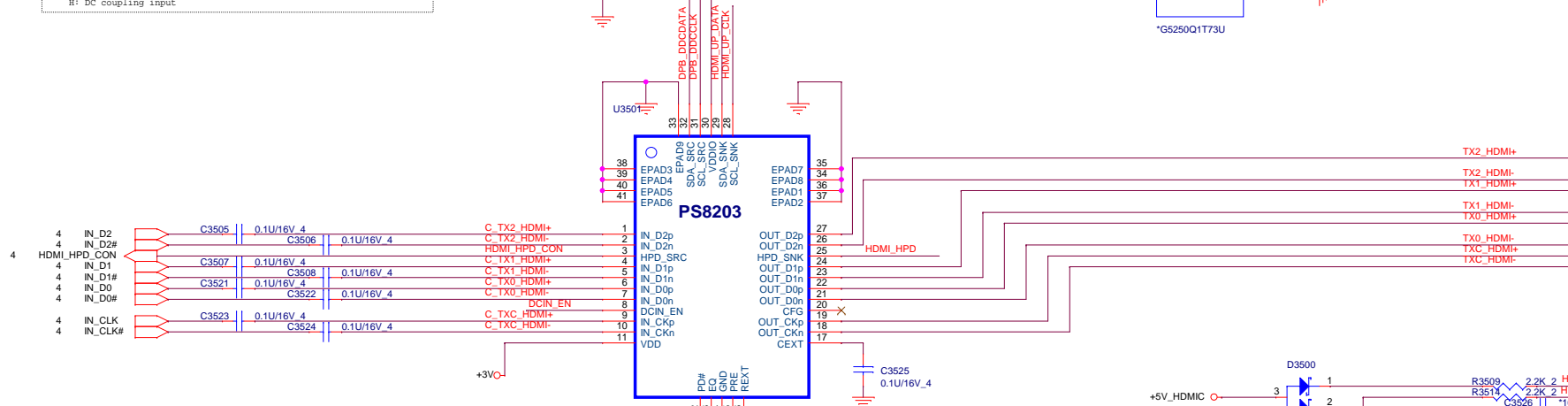
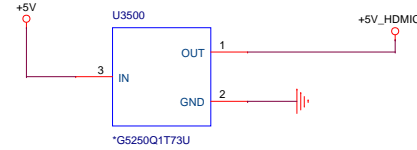
Output pre-emphasis setting; Internal pull down at ~150k Ω , 3.3V I/O.
L: no pre-emphasis
H: 2.5dB pre-emphasis

Receiver equalization setting; Internal pull down at ~150k Ω , 3.3V I/O.
L: programmable EQ for channel loss up to 12.4dB @ 3Gbps
H: programmable EQ for channel loss up to 4.3dB @ 3Gbps
M: programmable EQ for channel loss up to 8.6dB @ 3Gbps

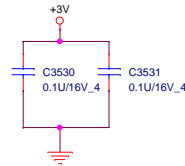
DC coupling enable; Internal pull down at ~150k Ω , 3.3V I/O.
L: default, AC coupling input
H: DC coupling input



for EMI request



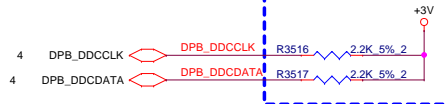
VDD for PS8203:
Power supply at 3.3V



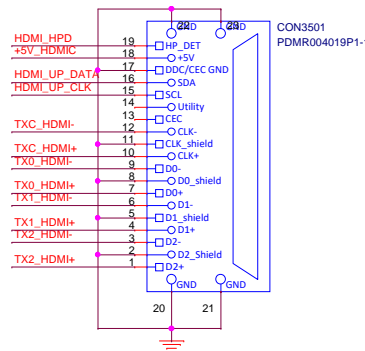
VDDIO:
Supply voltage for DDC passive gate and used to set HPD_SRC output level
Its range can be 1.2V~3.6V

HDMI SMBus Isolation

400 G8, 0225



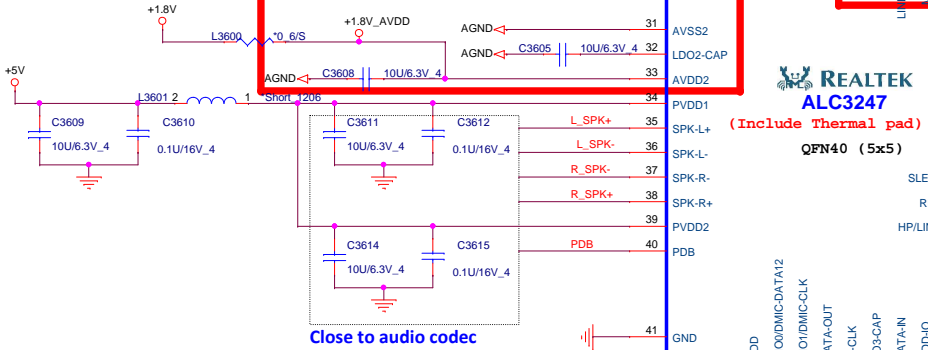
400 G8, 0219, 0226, 0528



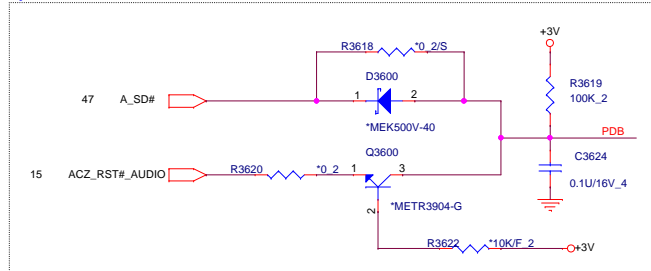
PROJECT : 400_600_G8
Quanta X8QA

Size Custom	Document Number 35 - HDMI CONNECTOR	Rev 3A
Date: Tuesday, July 21, 2020	Sheet 35of 106	

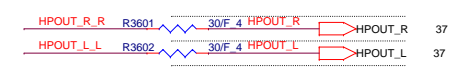
Audio Codec

ANALOG
DIGITAL

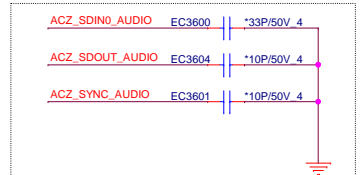
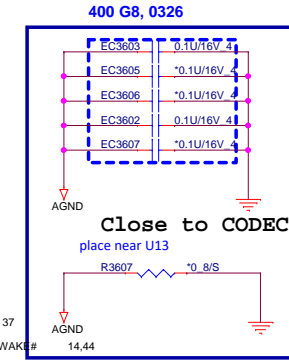
Speaker Power Down Control Circuit



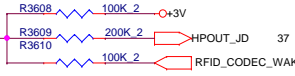
PCB trace width of SLEEVE & RING2 are required at least 40 mil and its length should be as short as possible



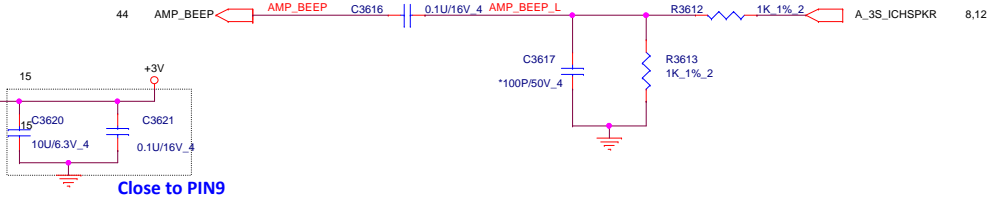
AGND SHIELD
AGND SHIELD TO Headphone jack
AGND SHIELD



Close to audio codec



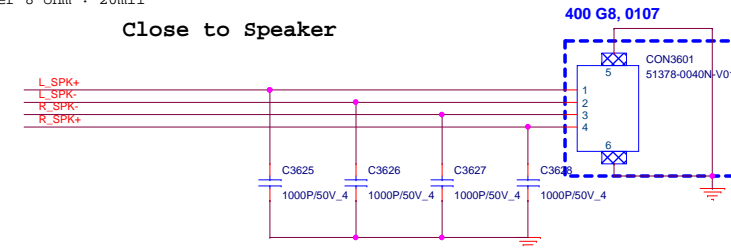
ANALOG
DIGITAL



Internal Speaker

Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil

Close to Speaker



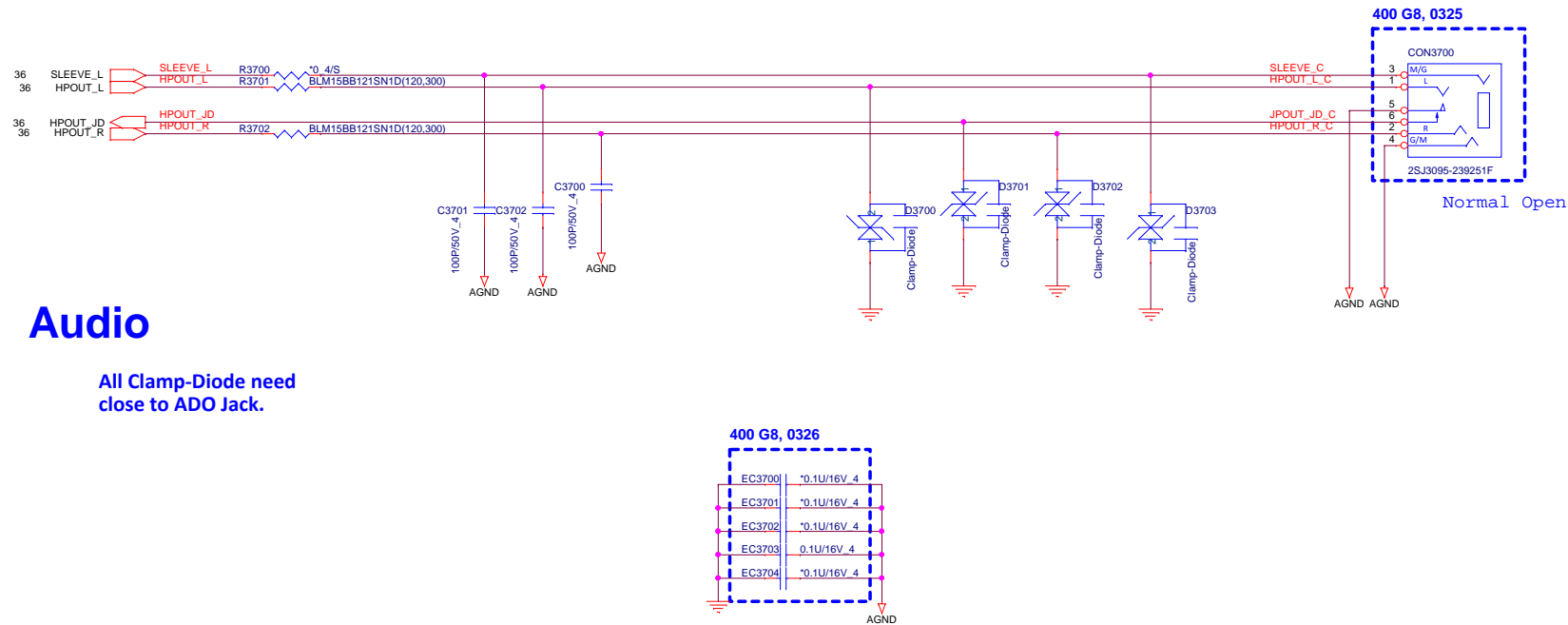
11,18,69,81,95
6,8,11,12,13,14,15,19,20,28,29,34,35,41,43,47,51,52,54,58,69,72,76,77,81,95,98,99
15,18,19,34,35,44,50,54,61,81,95

+1.8V
+3V
+5V



PROJECT : 400_600_G8
Quanta X8QA

Size Custom	Document Number 36 - Audio Codec CX7501	Rev 3A
Date: Tuesday, July 21, 2020	Sheet 36of	106



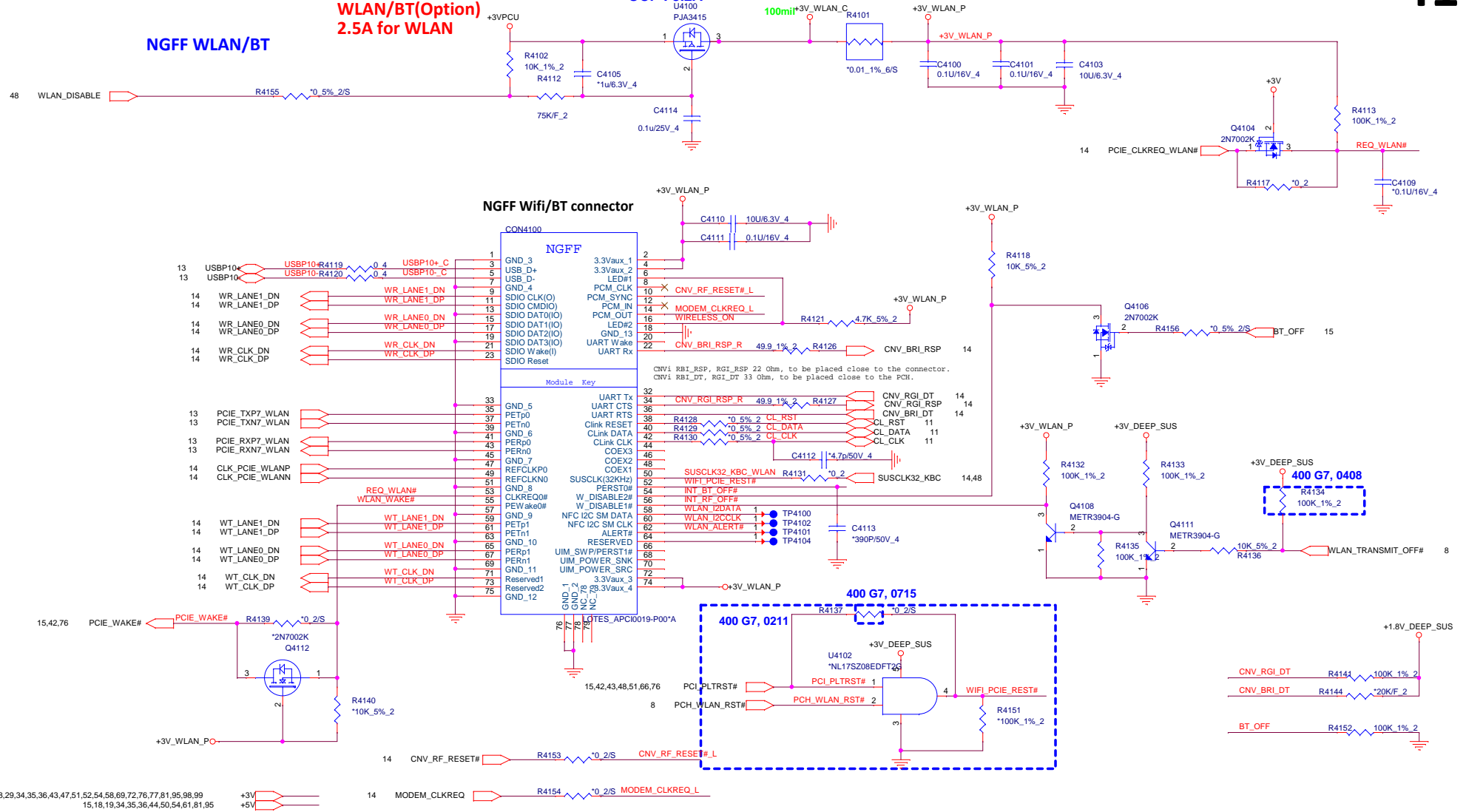
Audio

All Clamp-Diode need
close to ADO Jack.

**Mini Card
WLAN/BT(Optional)
2.5A for WLAN**

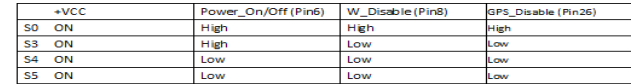
OCP : 3.2A

NGFF WLAN/BT



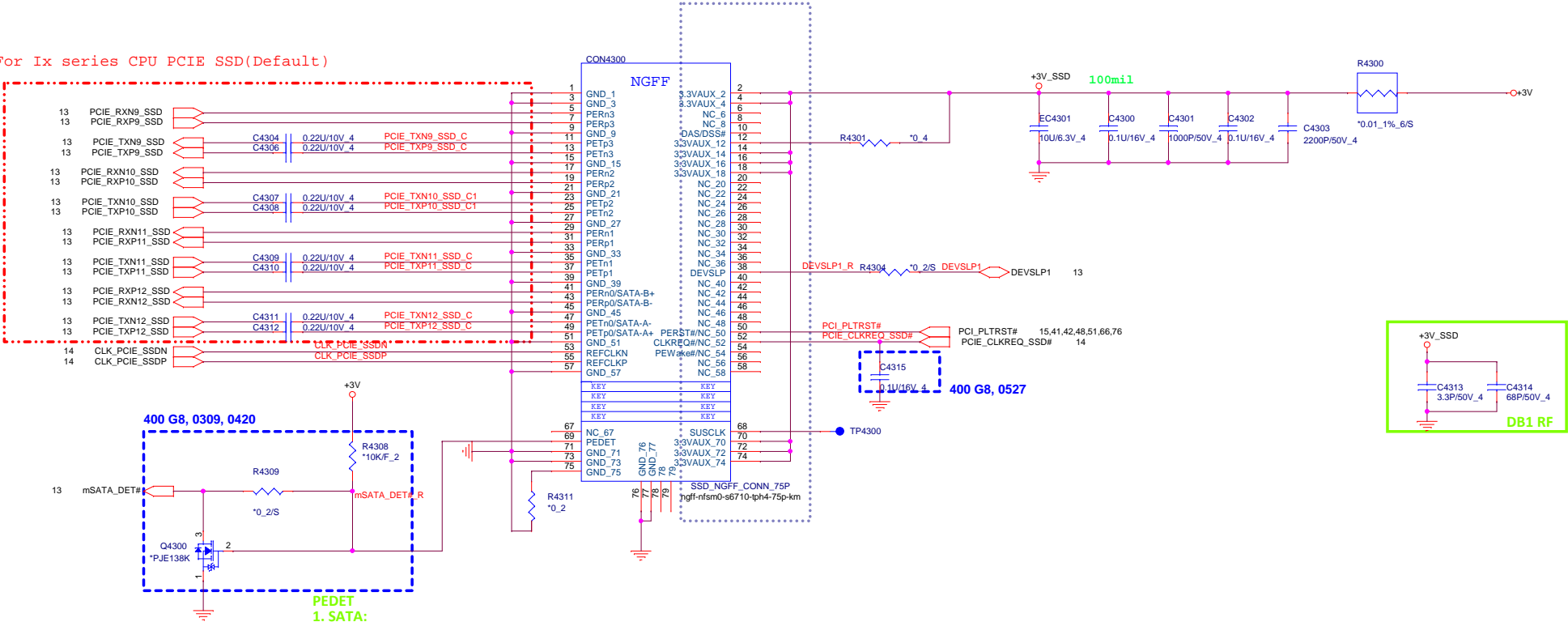
6,8,11,12,13,14,15,19,20,28,29,34,35,36,43,47,51,52,54,58,69,72,76,77,81,95,98,99
15,18,19,34,35,36,44,50,54,61,81,95

A diagram of a 2-to-1 multiplexer. It has two inputs on the left labeled +3V and +5V. These inputs are connected to a central diamond-shaped symbol representing the multiplexer. Two output lines extend to the right from the multiplexer.



600 Nano SIM :R4280,R4282,R4284,R4286,R4288 stuff
400 Internal SIM: R4281,R4283,R4285,R4287,R4289 stuff

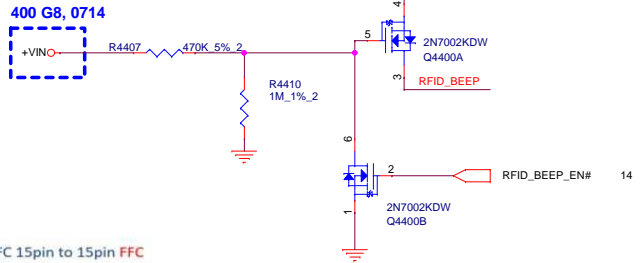
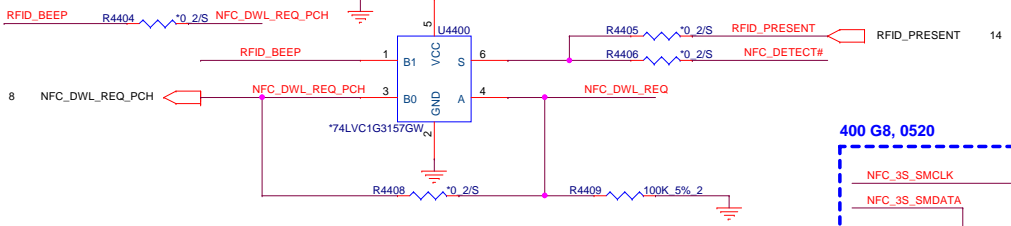
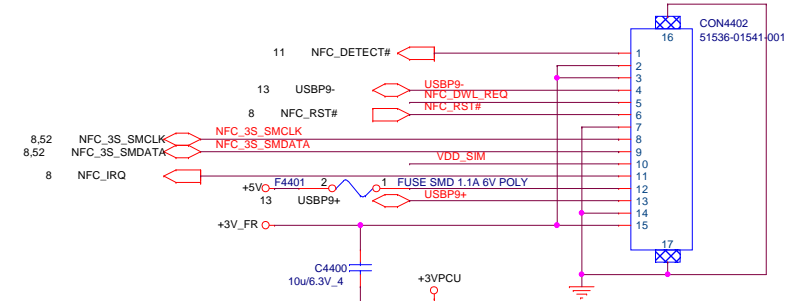
For Ix series CPU PCIE SSD(Default)



6,8,11,12,13,14,15,19,20,28,29,34,35,36,41,47,51,52,54,58,69,72,76,77,81,95,98,99

+3V

NFC/RFID
NFC
Address: 0x2XX(7 bit)



- 1. NFC 15pin to 15pin FFC
- 2. RFID 15pin to 10pin FPC

Pinout Tables

MODULE CONNECTOR (RFID)

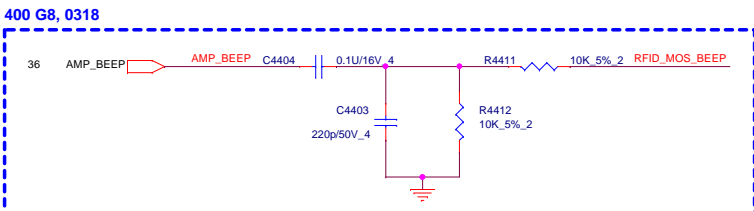
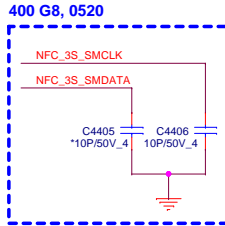
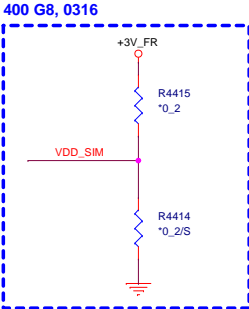
Table with 2 columns: Pin number, Name. Rows 1-10 detailing pin functions for the module connector.

HOST CONNECTOR

Table with 3 columns: Pin number, Host NFC/RFID Connector, Note. Rows 1-15 detailing pin functions for the host connector.

****RFID module pin1 is a multiple-function pin but is NOT used in HP platforms. For FPC design, do NOT connect this pin to host connector pin15 (just left open).

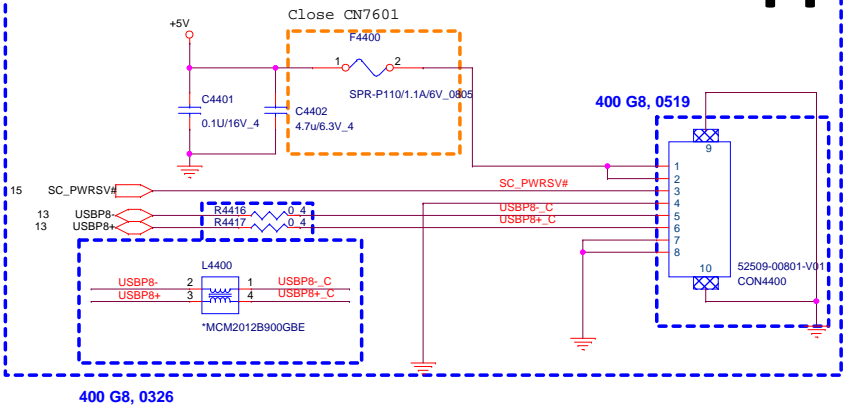
*NFC_IRQ will be re-purposed to signal host to flash keyboard backlight with RFID module installed.



6,8,11,12,13,14,15,19,20,28,29,34,35,36,41,43,47,51,52,54,58,69,72,76,77,81,95,98,99

SMART CARD

44



NTAG Conn

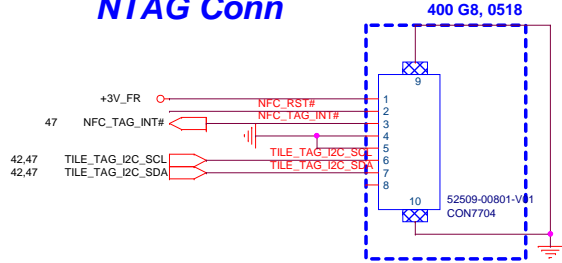
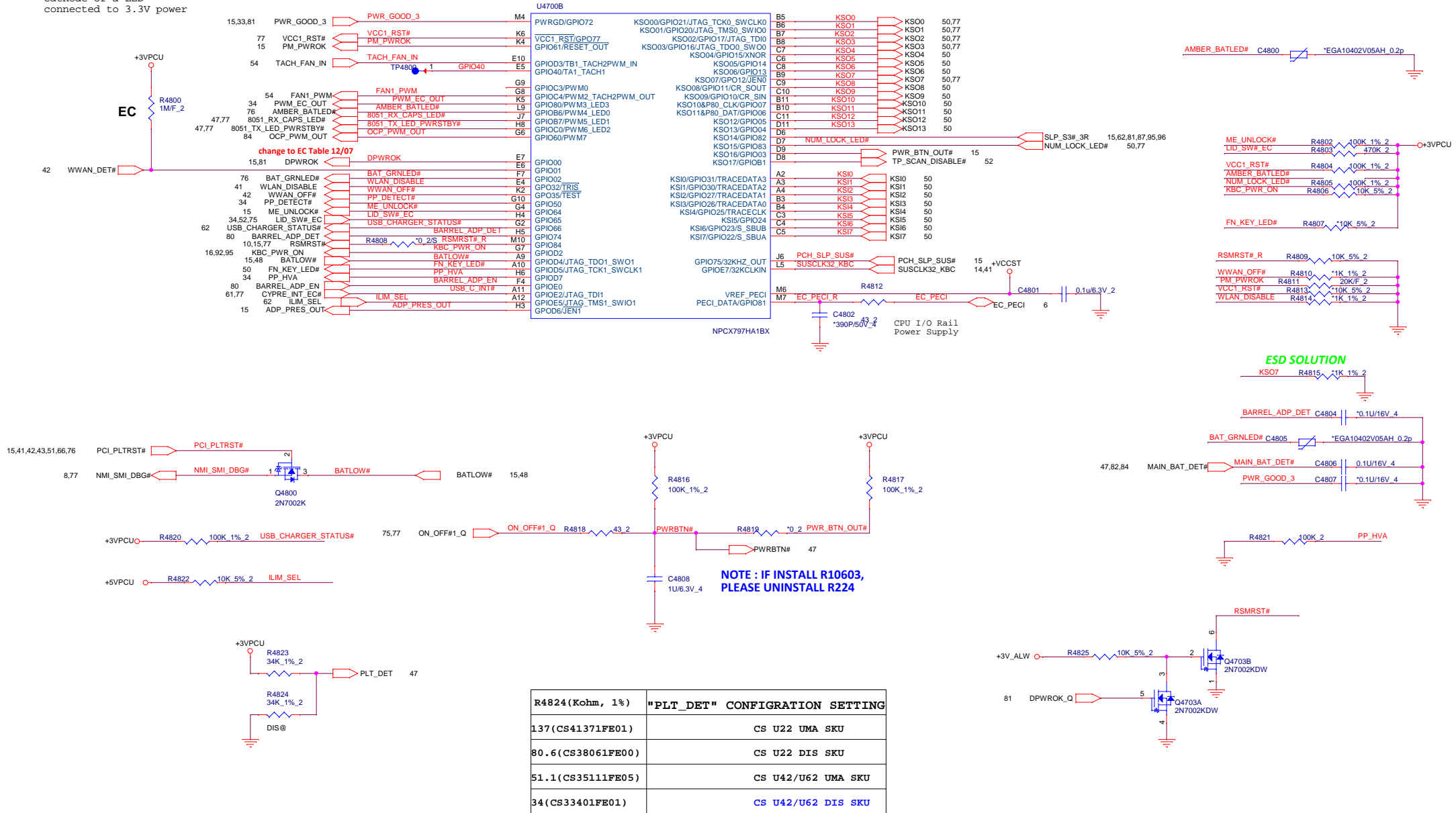


Table with 3 columns: Pin, Symbol, Description. Rows 1-8 detailing pin functions for the NTAG connection.

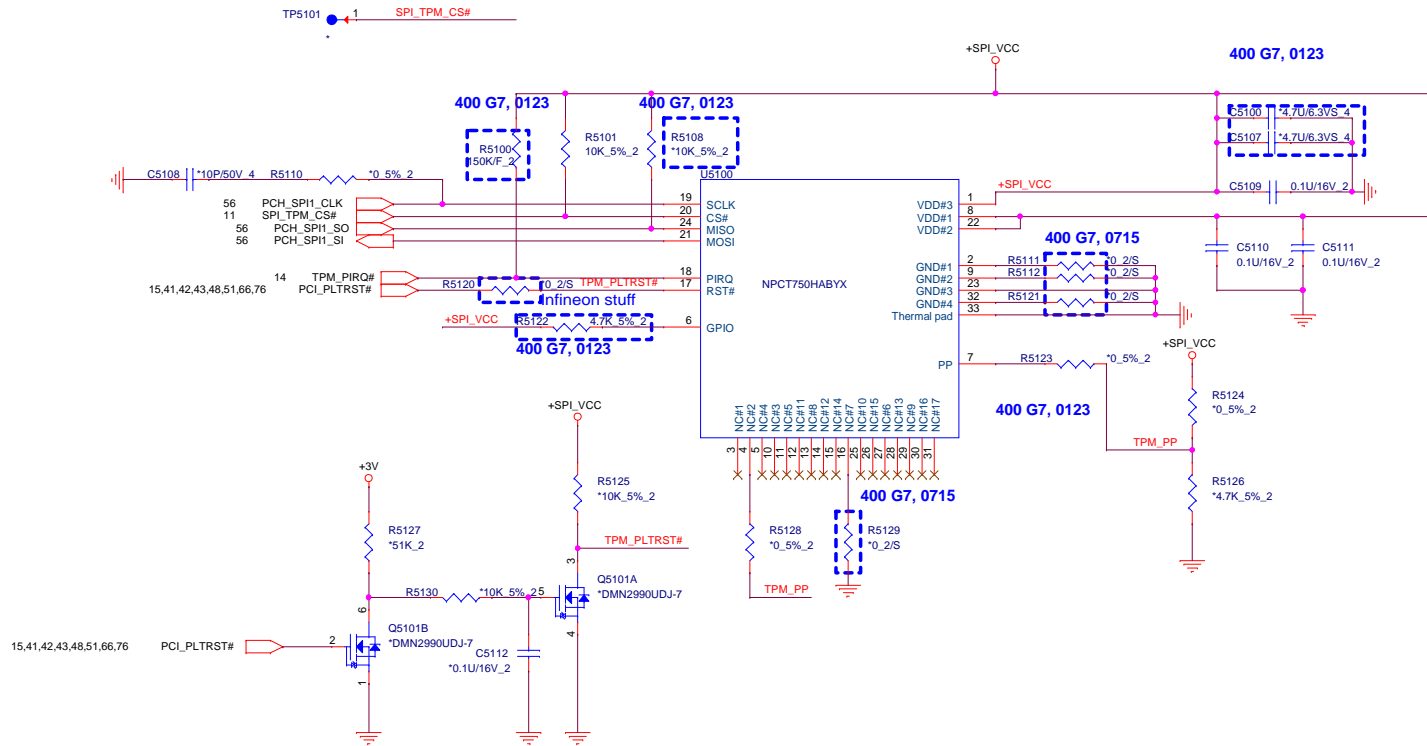


PROJECT : 400_600_G8
Quanta X8QA

All the PWM outputs can directly drive the cathode of a LED connected to 3.3V power



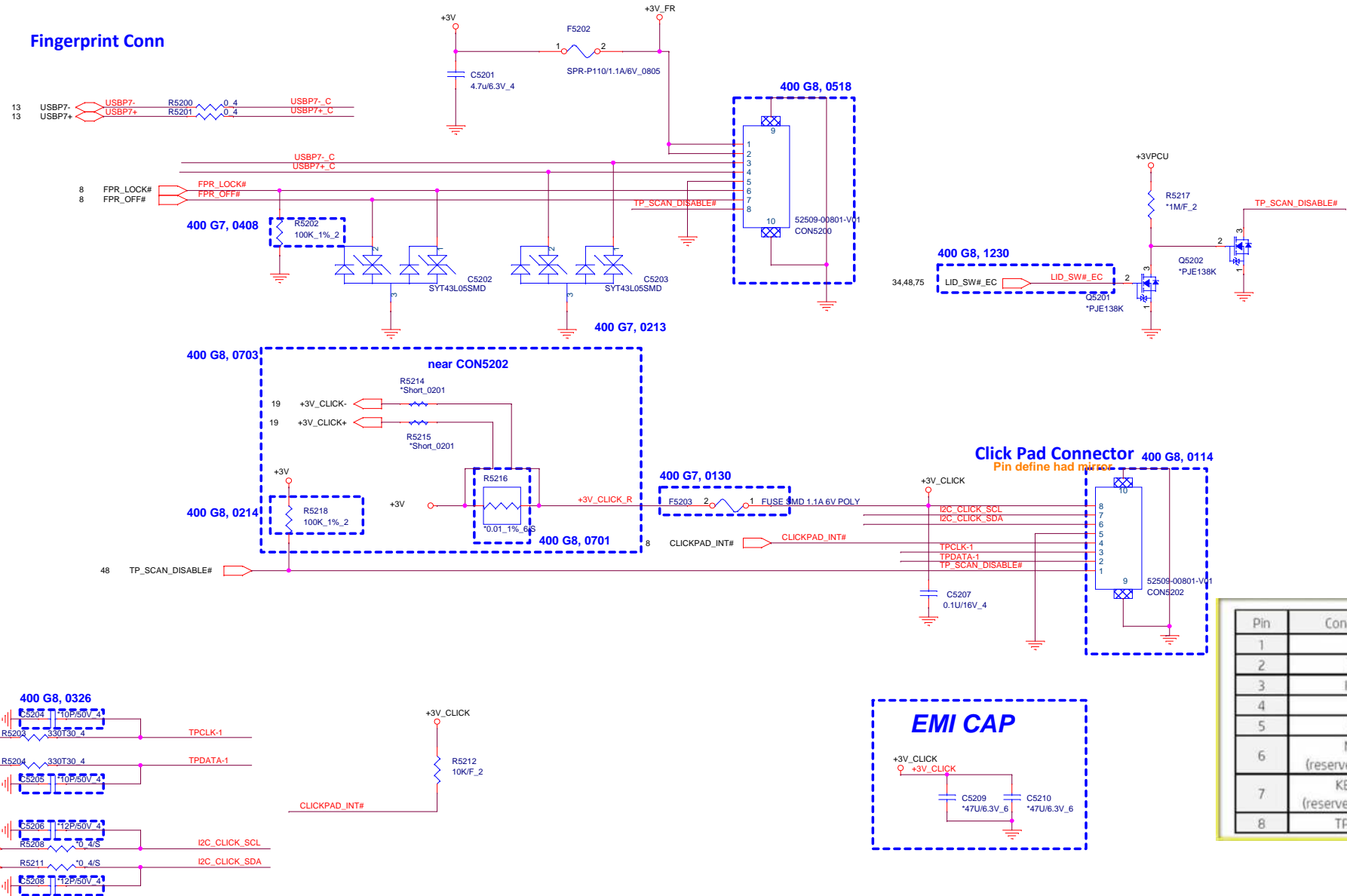
TPM (1.2 or 2.0)



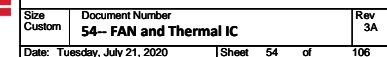
AL000750004 AL009670041
AL000750008--MV AL009670042-MV

	Nuvoton	Infineon
C5106	V	
C5105	V	
R5116	V	
R5113	V	
R5115	V	
R5117		V
R5118		V
R5119		V
R5114		V
R5104		V
R5100	10K	150K

Fingerprint Conn



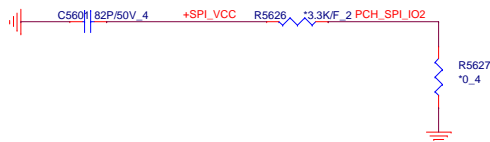
CLICK PAD
Address: 0x20(7 bit)



400 G8, 0319

SPI ROM

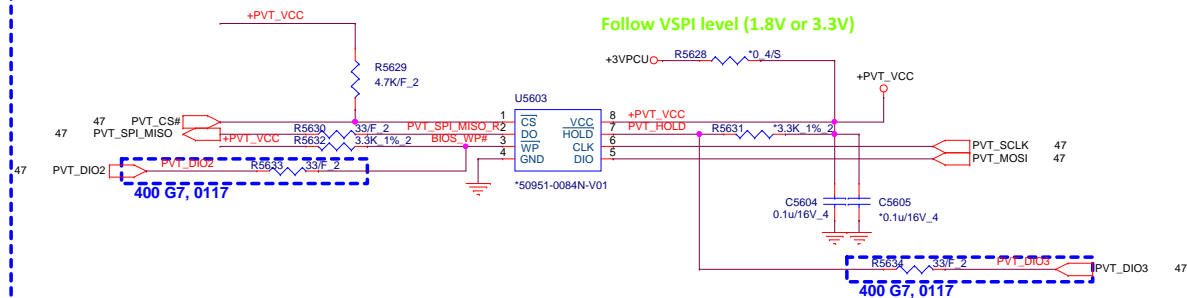
Vender	Size	P/N
MXIC	32MB	AKE3JZ-KZ01
Winbond	32MB	AKE3JF00N00
Socket		DFHS08FS060

PCH SPI ROM(CLG)
Place TP at TOP side

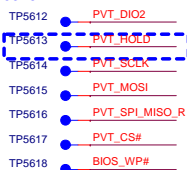
400 G8, 0305

EC SPI ROM Socket WSON 16M 6x5

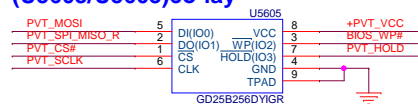
Follow VSPI level (1.8V or 3.3V)



400 G8, 0319



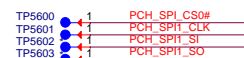
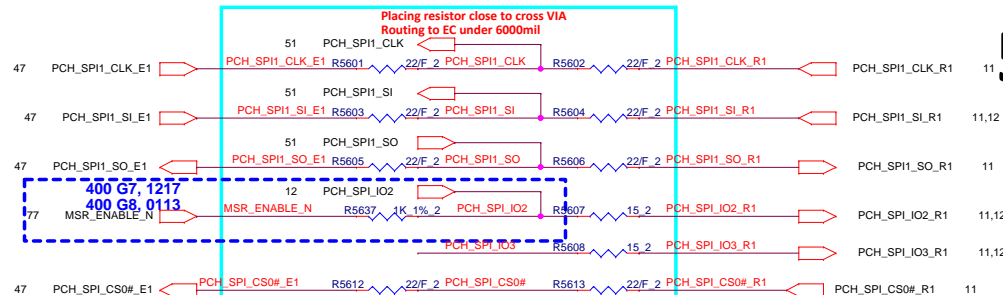
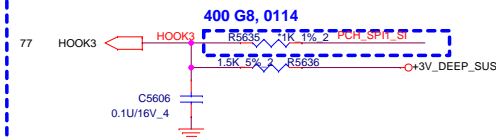
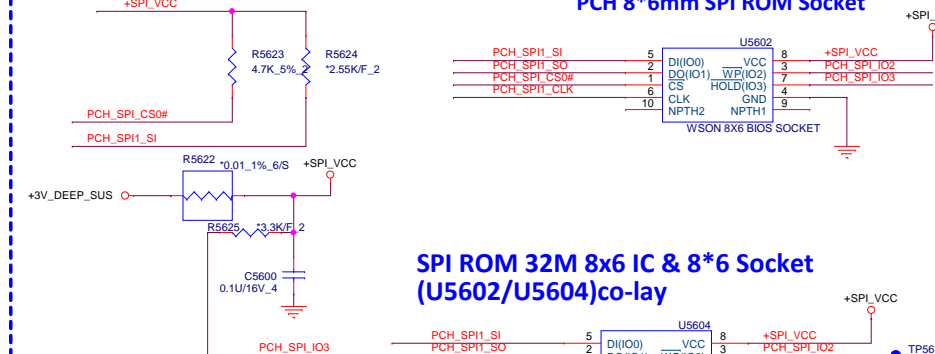
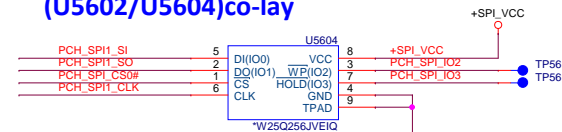
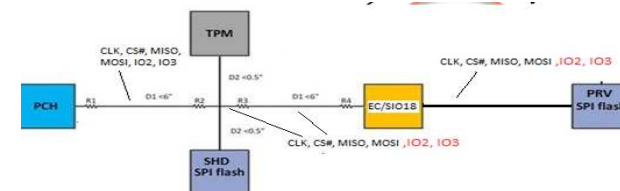
400 G8, 0304

Reserve EC SPI ROM 32M Byte (U5603/U5605)co-lay

400 G8, 0319

EC SPI ROM

Vender	Size	P/N
GGD	32MB	AKE3JZ00Q02

MV/MP stuff**BIOS SPI ROM 32M Byte PCH 8*6mm SPI ROM Socket****SPI ROM 32M 8x6 IC & 8*6 Socket (U5602/U5604)co-lay****PCH 8*6mm WSON 32M**

nuvoton

Nuvoton Confidential - Provided under NDA

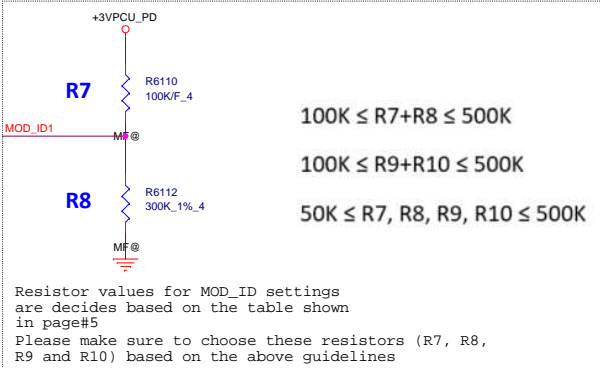
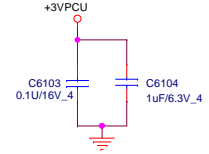
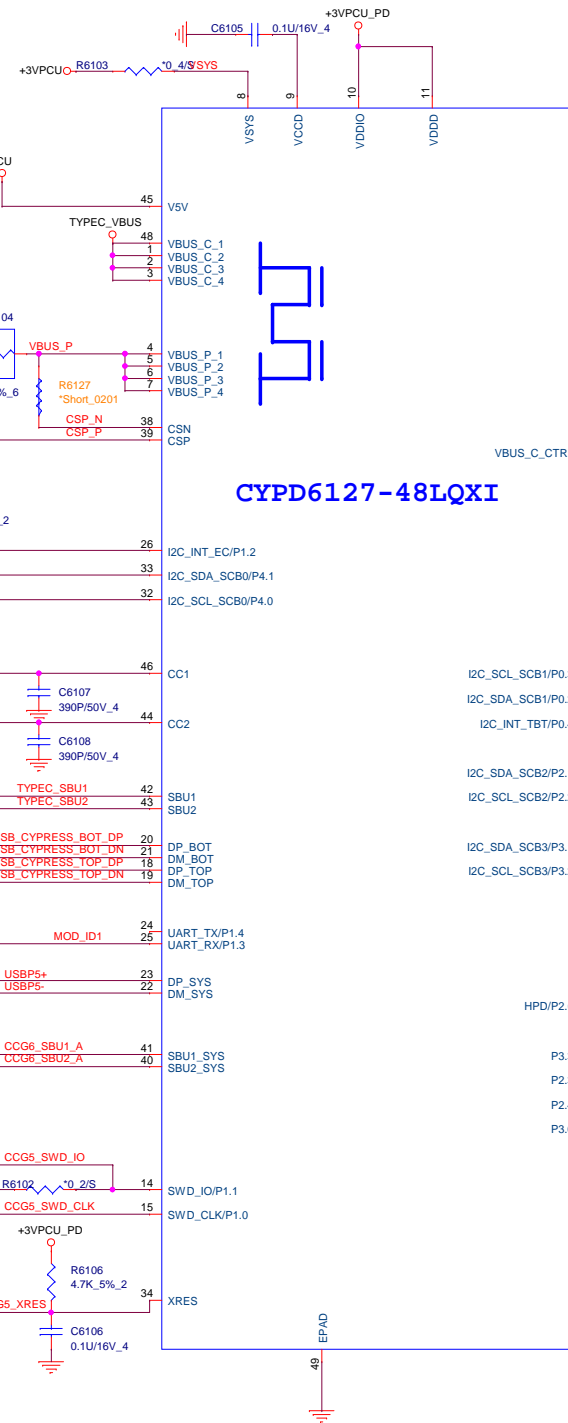
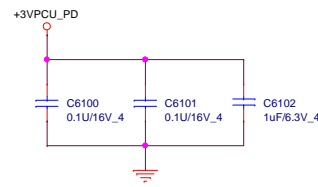
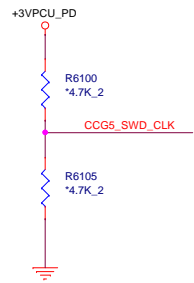
Based on EC18 testing: PCH to TPM/SPI flash = Quad I/O, SIO18 to SPI Flash = Quad I/O.
 R1 = 4.7 ohm for CLK, CS#, MISO, MOSI; R1 = 0 ohm for IO2, IO3
 R2 = 22 ohm for CLK, CS#, MISO, MOSI; R2 = 15 ohm for IO2, IO3
 R3 = 22 ohm for CLK, CS#, MISO, MOSI; R3 = 22 ohm for IO2, IO3
 R4 = 4.7 ohm for CLK, CS#, MISO, MOSI; R4 = 4.7 ohm for IO2, IO3

Note: The value of the resistors should be tuned according to the signal integrity simulations or actual PCB measurements.



PROJECT : 400_600_G8
Quanta X8QA

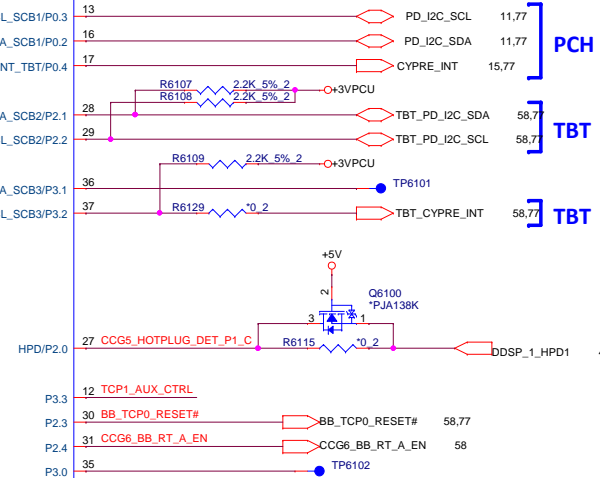
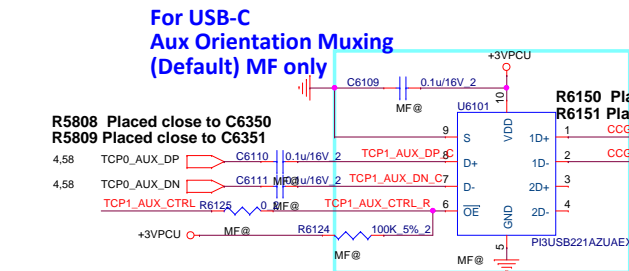
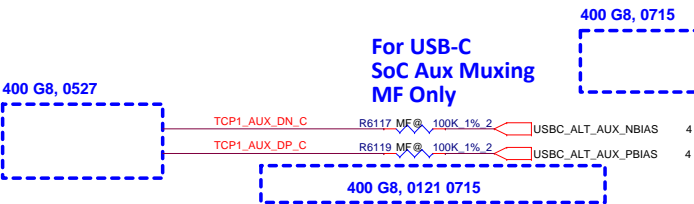
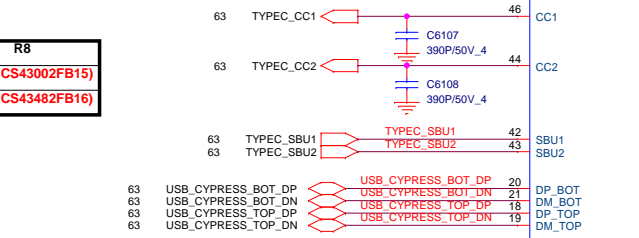
Size	Document Number	Rev
Custom	56 - Flash(KBC+PCH)	3A
Date: Tuesday, July 21, 2020	Sheet	56 of 106



Platform ID	MOD_ID1	MOD_ID2	Description	CCG6SF	I/O
MOD_ID1	MOD_ID2				
L7	X	X	DRP + USB4		L1 = VDD0/8
L6	X	X	DRP + DP (MF)		L2 = 2* VDD0/8
L5	X	X	Reserved		L3 = 3* VDD0/8
L4	X	X	Reserved		L4 = 4* VDD0/8
L3	X	X	Reserved		L5 = 5* VDD0/8
L2	X	X	Reserved		L6 = 6* VDD0/8
L1	X	X	Reserved		L7 = 7* VDD0/8
					L8 = VDD0

R7	R8
L6(MF) 100K(CS41002FB28)	300K(CS43002FB15)
L7(TBT) 50K(CS35102JB14)	350K(CS43482FB16)

EC

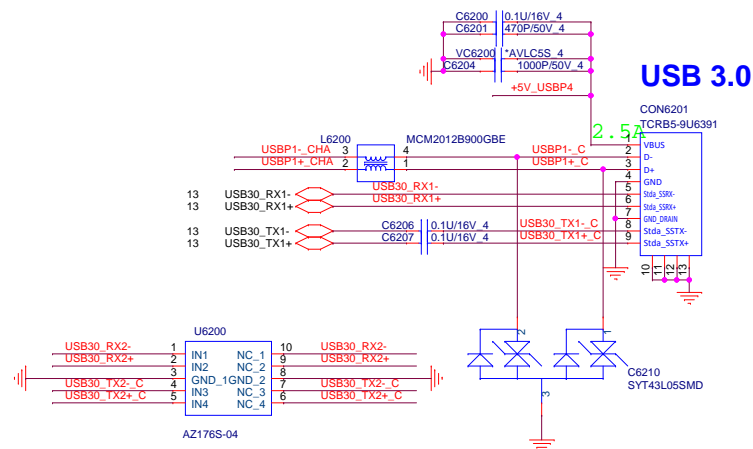


PROJECT : 400_G8
Quanta X8QA

USB Charging Port

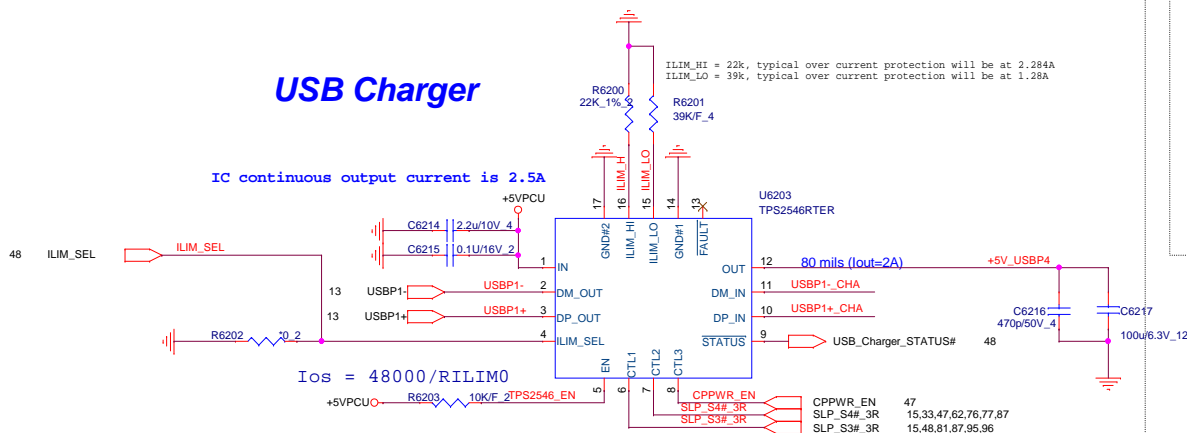


USB 2.0/3.0 Combo Right for Charge

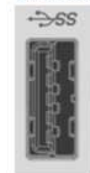


USB Charger

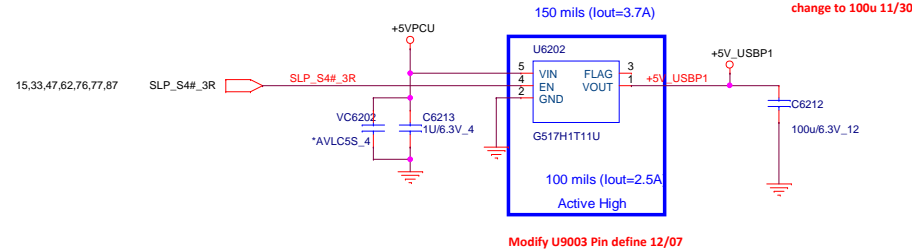
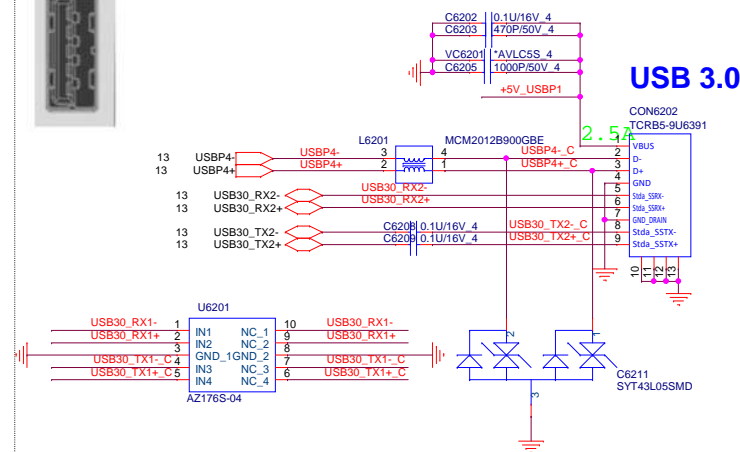
IC continuous output current is 2.5A



USB Stander Port

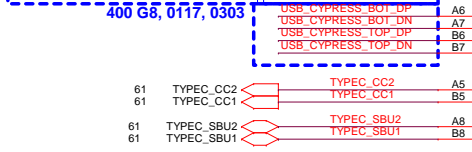
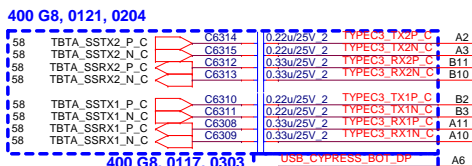
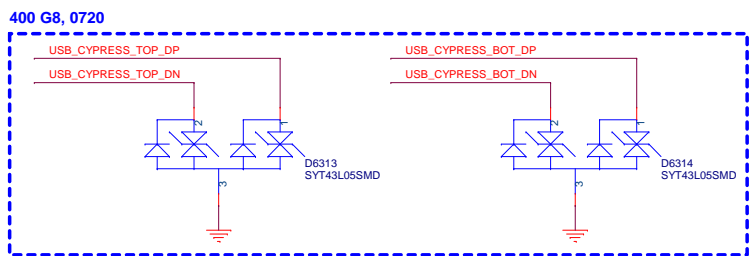
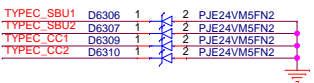
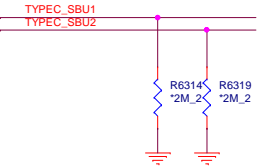
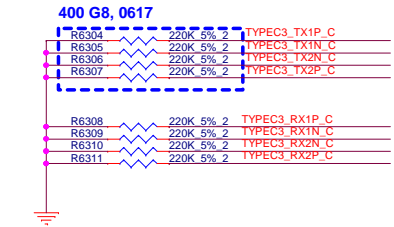
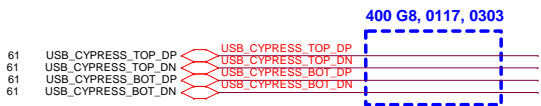


USB 2.0/3.0 Combo

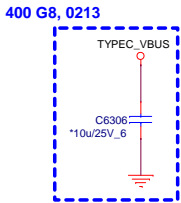
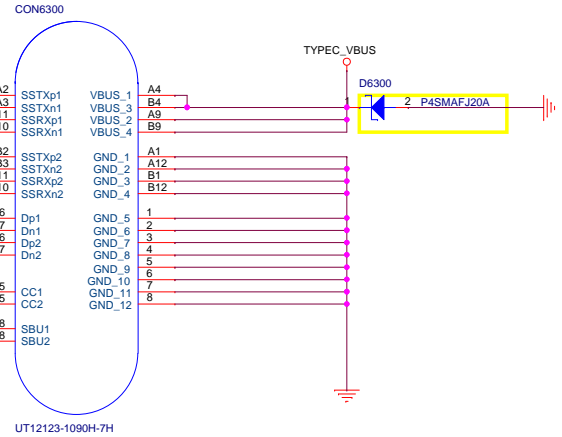


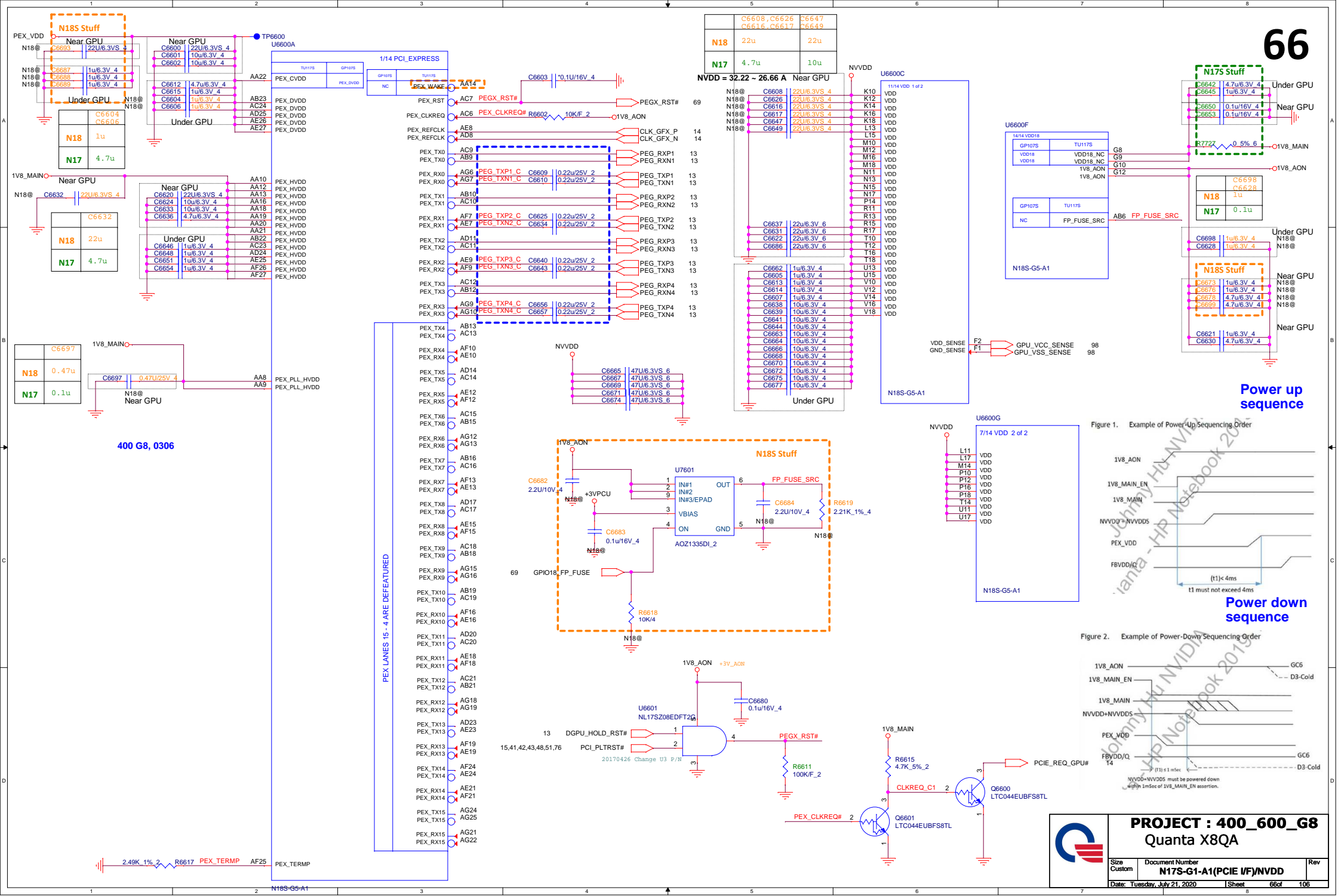
USB Type-C Port A

65W, 20V, 3.25A
130MIL

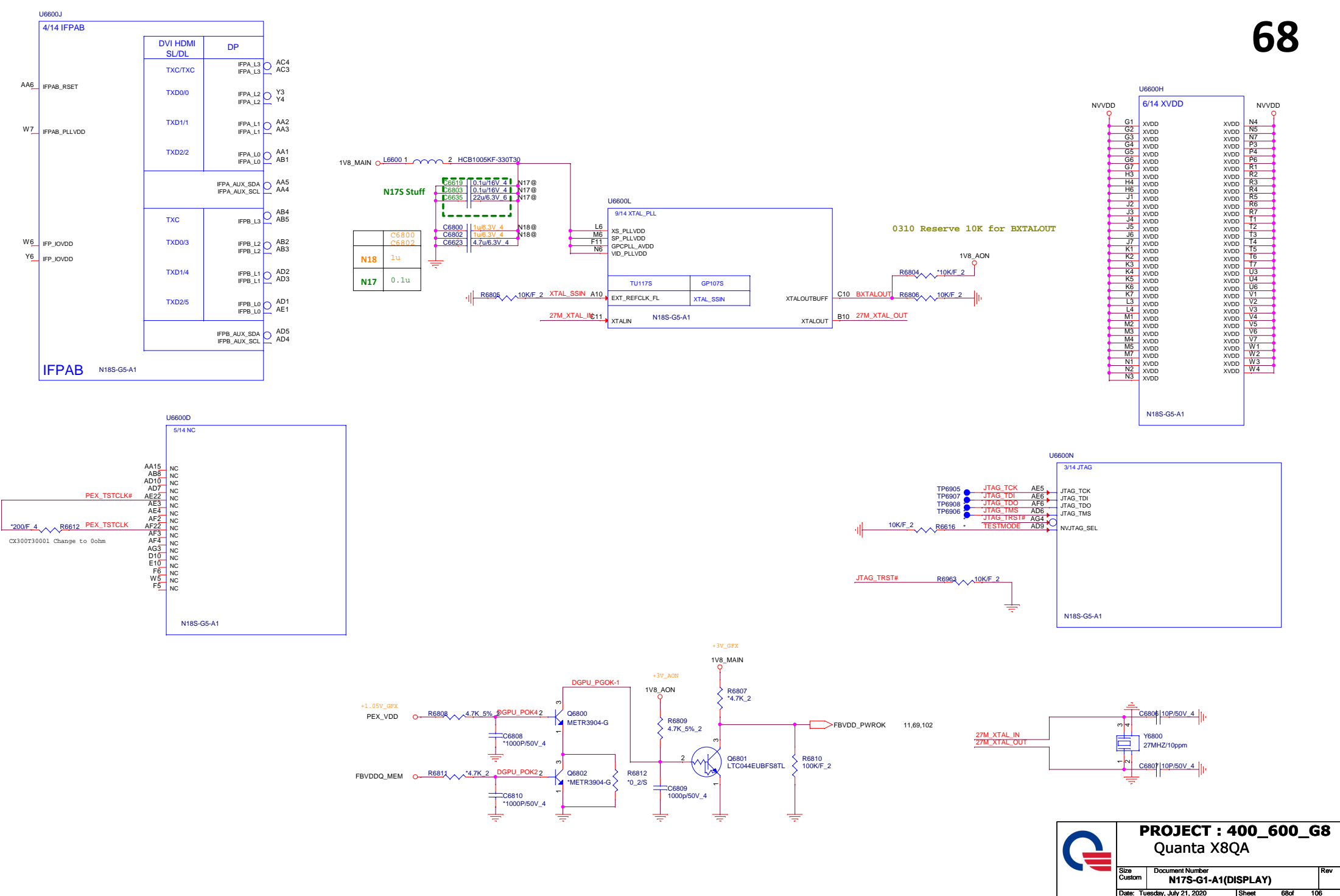


Note : PD can use common FW
and don't need to swap for USB2.0







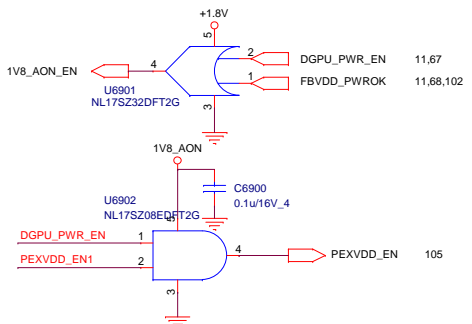




RAMCFG [2:0]	DESCRIPTION	Vendor	Vendor P/N	TOP P/N	QB P/N
0x4	GDDR5 256Mx32 8 GHz	Samsumg C die	K4G80 325FC-HC25	AKG5QGUT501	AKG5QGUT500
0x1	GDDR5 256Mx32 8 GHz	Micron B die	MT51J256M32HF-80:B	AKG5QGUTL24	AKG5QGUTL27
0x2	GDDR5 256Mx32 8 GHz	Hynix A die	H5GC8B24AJR-R2C	AKG5QGUTW15	AKG5QGUTW18

STRAP[2:0] VRAM Table for N17S-G5-A1 GDDR5 Recommended Memories					
RAMCFG [2:0]	DESCRIPTION	Vendor	Vendor P/N	TOP P/N	QB P/N
0xB	GDDR5 256Mx32 8 GHz	Samsung C die	K4G80325FC-HC25	AKG5QGUT501	AKG5QGUT500
0x9	GDDR5 256Mx32 8 GHz	Micron B die	MT51J256M32BF-80:B	AKG5QGUTL24	AKG5QGUTL27
0xA	GDDR5 256Mx32 8 GHz	Hynix A die	H5GC8H24AJR-R2C	AKG5QGUTW15	AKG5QGUTW18

	Description	Size	P/N
N18S	GD25LQ80CTIGR	8Mb	AKE5GF00Q01
	MX25U8033EM1I-12G	8Mb	AKE5GFP0Z02




	PROJECT : 400_600_G8 Quanta X8QA		
	Size Custom	Document Number N17S-G1-A1(GPIO/STRAPS)	Rev
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Table 9.5 GDDR5 DEBUG Command Lines

Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

Table 9.4 GDDR5 Command Mapping (GB4C-128 & GB2C-64 packages)

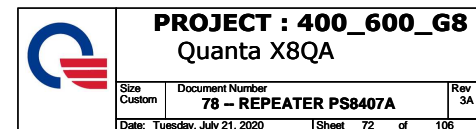
Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

Table 15-2. Resistance Mapping to Hex Values

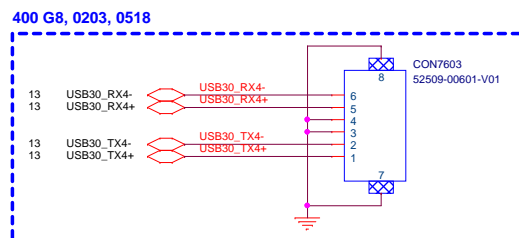
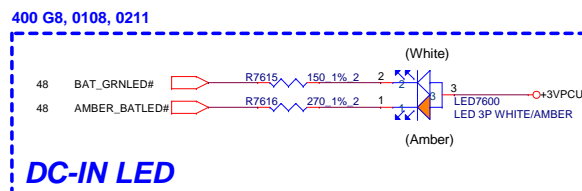
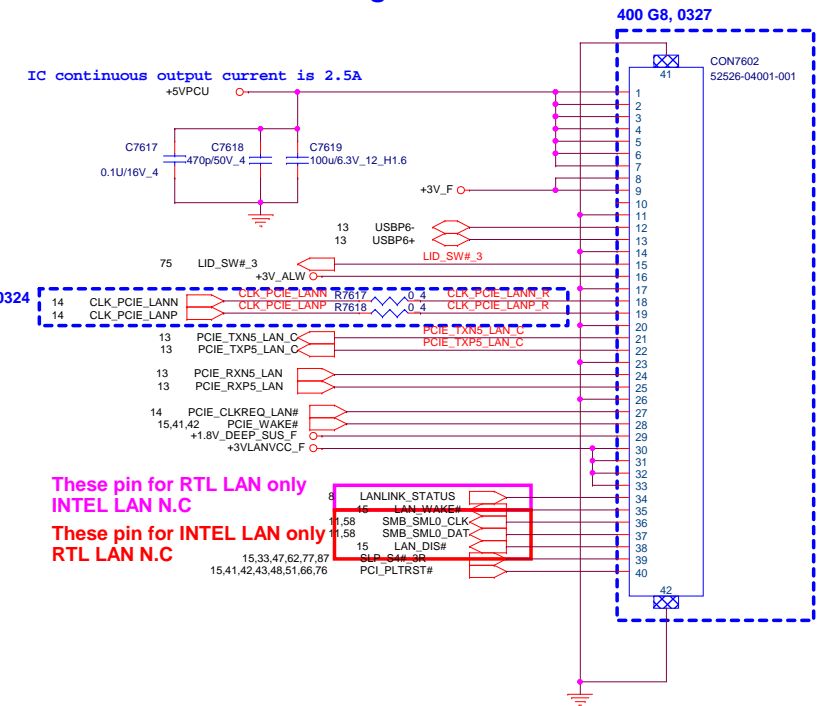
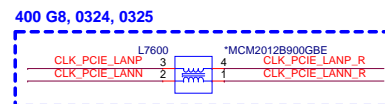
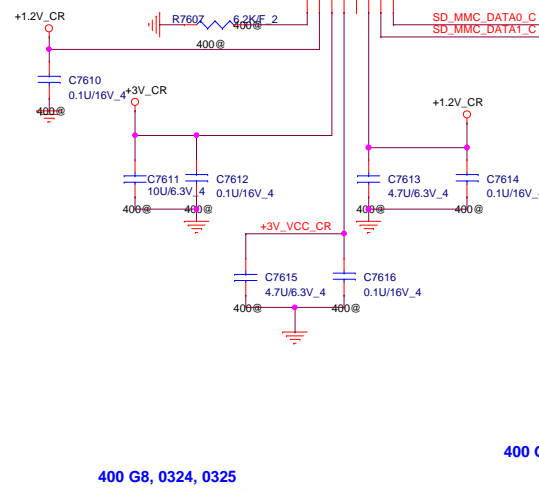
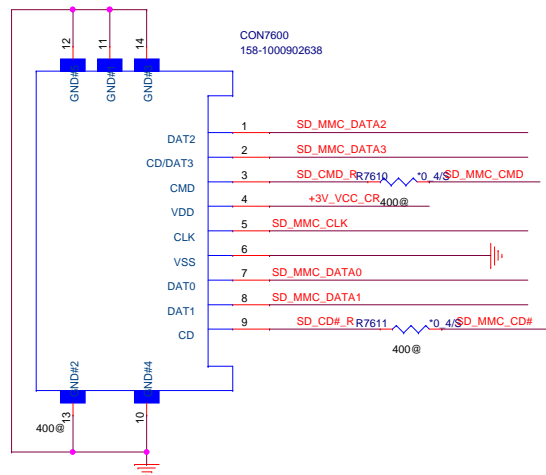
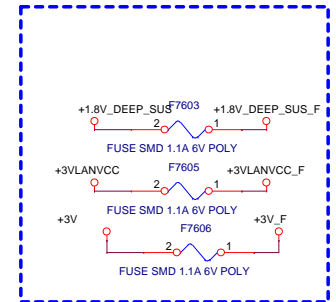
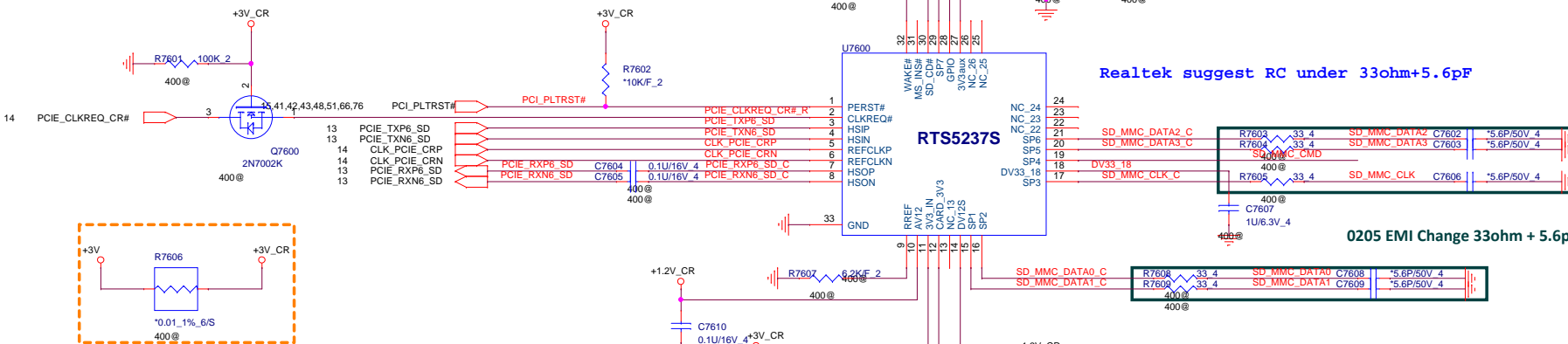
Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

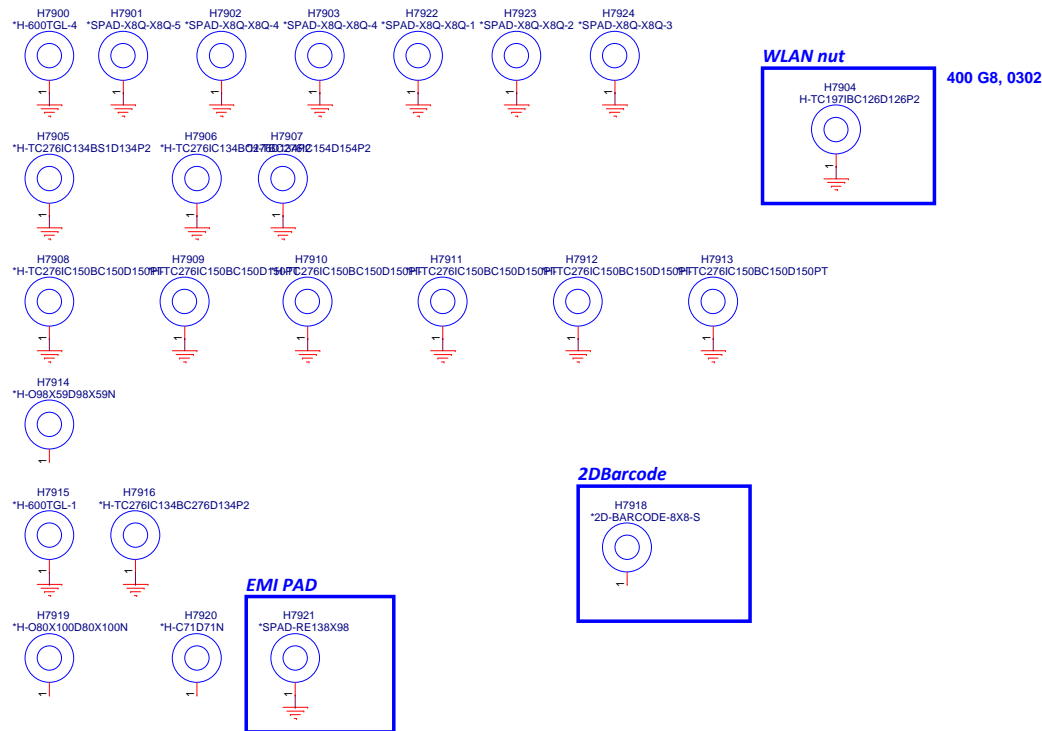
Table 4. N17S-LG/-G1 GDDR5 Recommended Memories

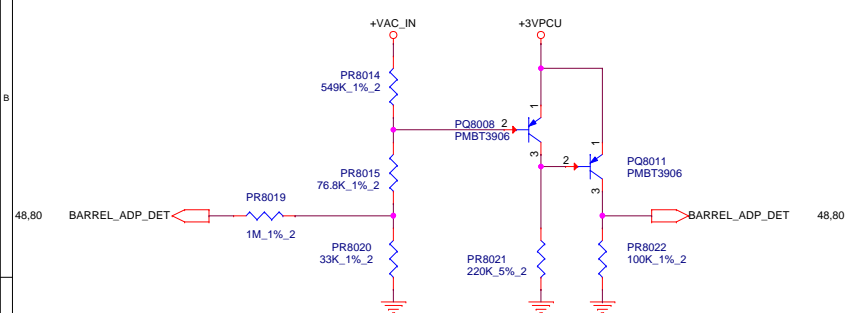
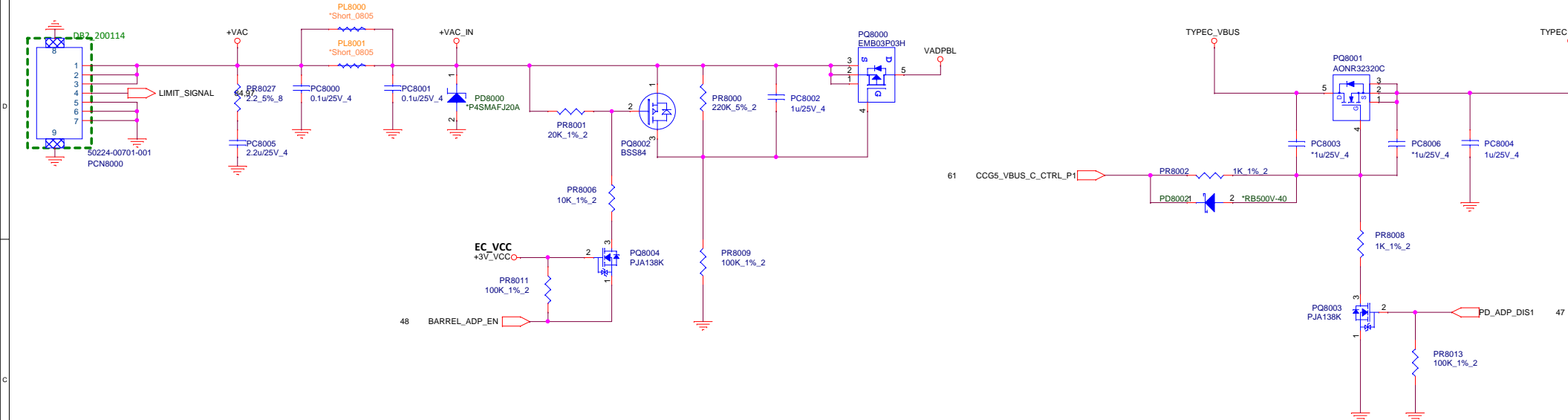
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production candidate
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production candidate
4 Gb	128Mx32	1.35V	Hynix	H5GC4H24AJR-R0C	A-die	0x6	7 Gbps	N/A	Full	Production candidate
			Samsung	K4G41325FE-HC28	E-die	0x7	7 Gbps	N/A	Full	Production candidate
			Micron	EDW4032BABG-70-F	A-die	0x8	7 Gbps	N/A	Full	Post production candidate



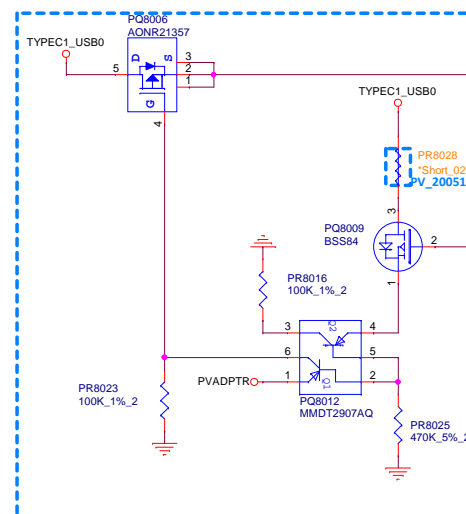




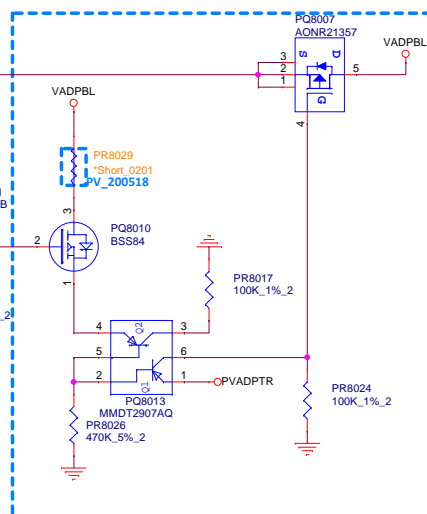


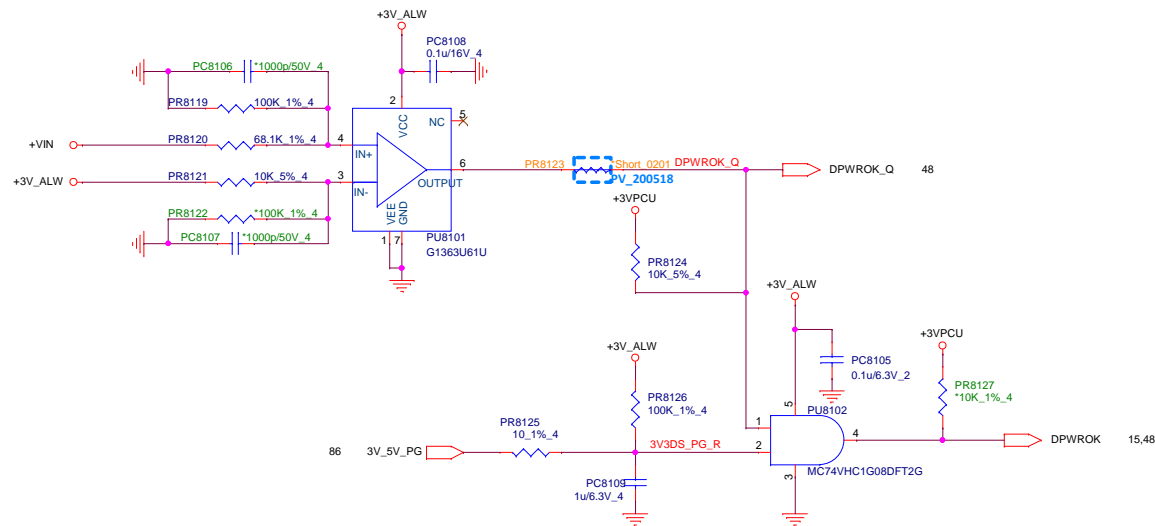
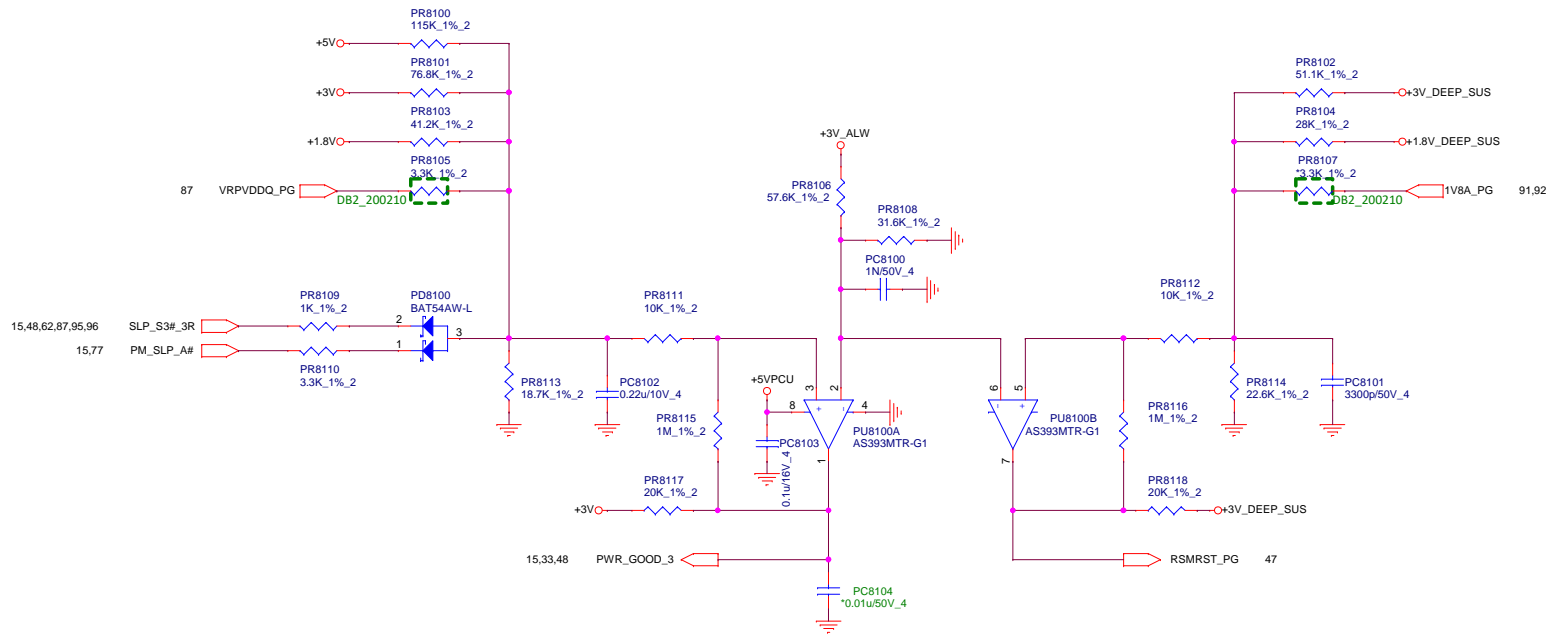


For Type-C Port 1



For Barrel Adapter



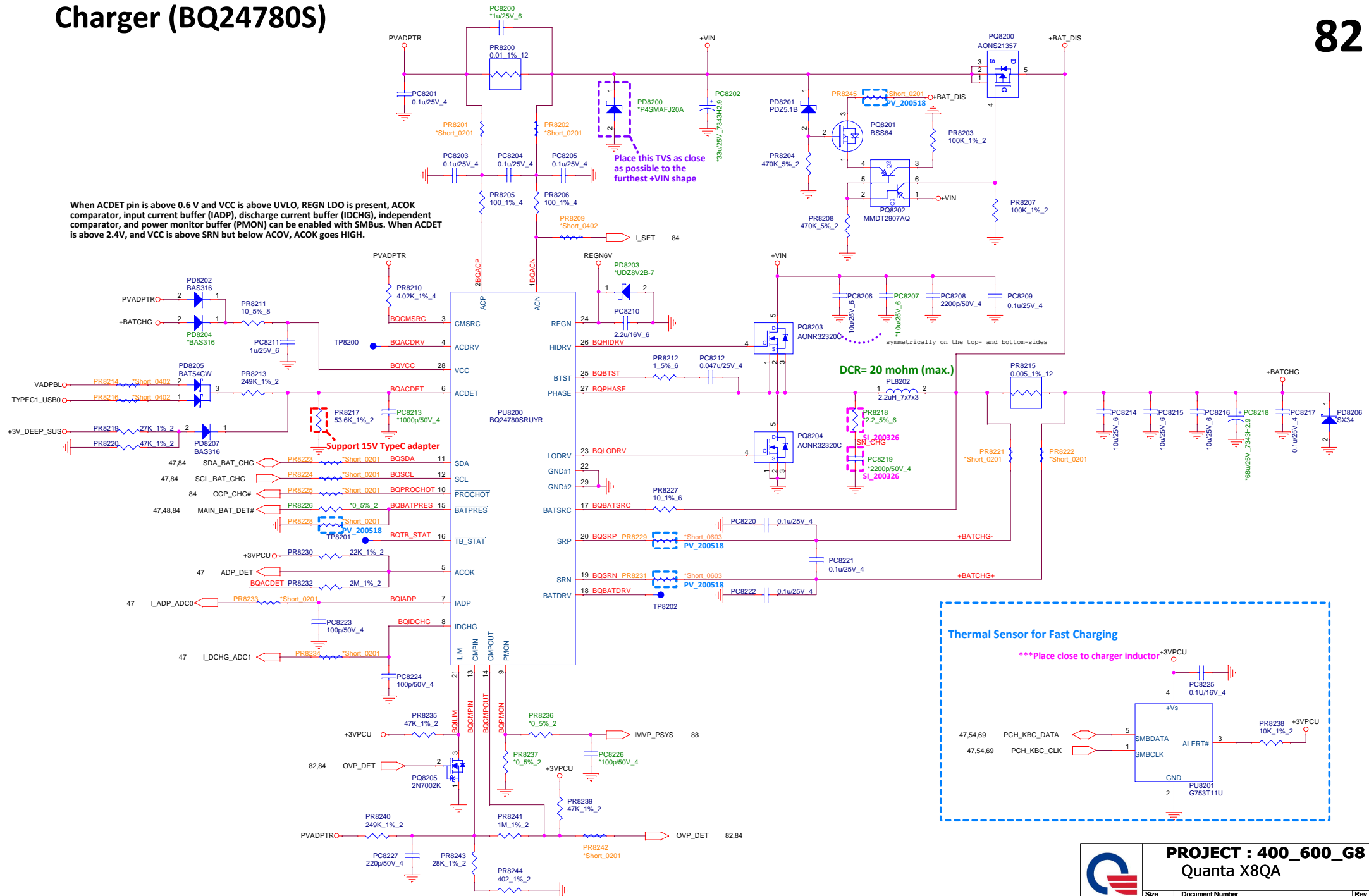



8,10,15,16,18,19,33,34,36,41,42,44,47,48,50,52,54,56,58,61,66,72,75,76,77,80,82,84,86,87,88,91,92,95,96,105	20,34,44,72,82,86,87,89,91,92,97,99,102	+VIN
8,11,12,14,15,16,19,41,42,47,72,76,77,92,95,105	11,18,36,69,95	+3VPCU
4,5,6,8,10,11,12,13,14,15,16,19,20,41,42,47,56,58,77,82,95	11,18,36,69,95	+3V_DEEP_SUS
6,8,11,12,13,14,15,19,20,28,29,34,35,36,41,43,47,51,52,54,58,69,72,76,77,95,98,99	15,18,19,34,35,36,44,50,54,61,95	+1.8V
	14,33,48,75,76,86,87	+3V
		+5V
		+3V_ALW

Charger (BQ24780S)

82

When ACDET pin is above 0.6 V and VCC is above UVLO, REGN LDO is present, ACOK comparator, input current buffer (IADP), discharge current buffer (IDCHG), independent comparator, and power monitor buffer (PMON) can be enabled with SMBus. When ACDET is above 2.4V, and VCC is above SRN but below ACOV, ACOK goes HIGH.



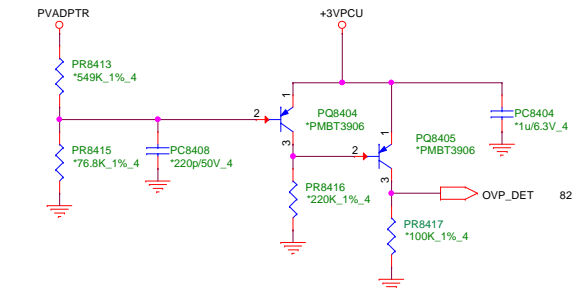
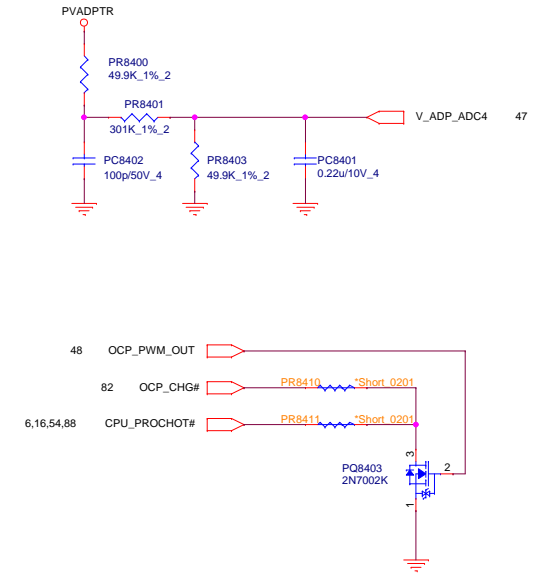
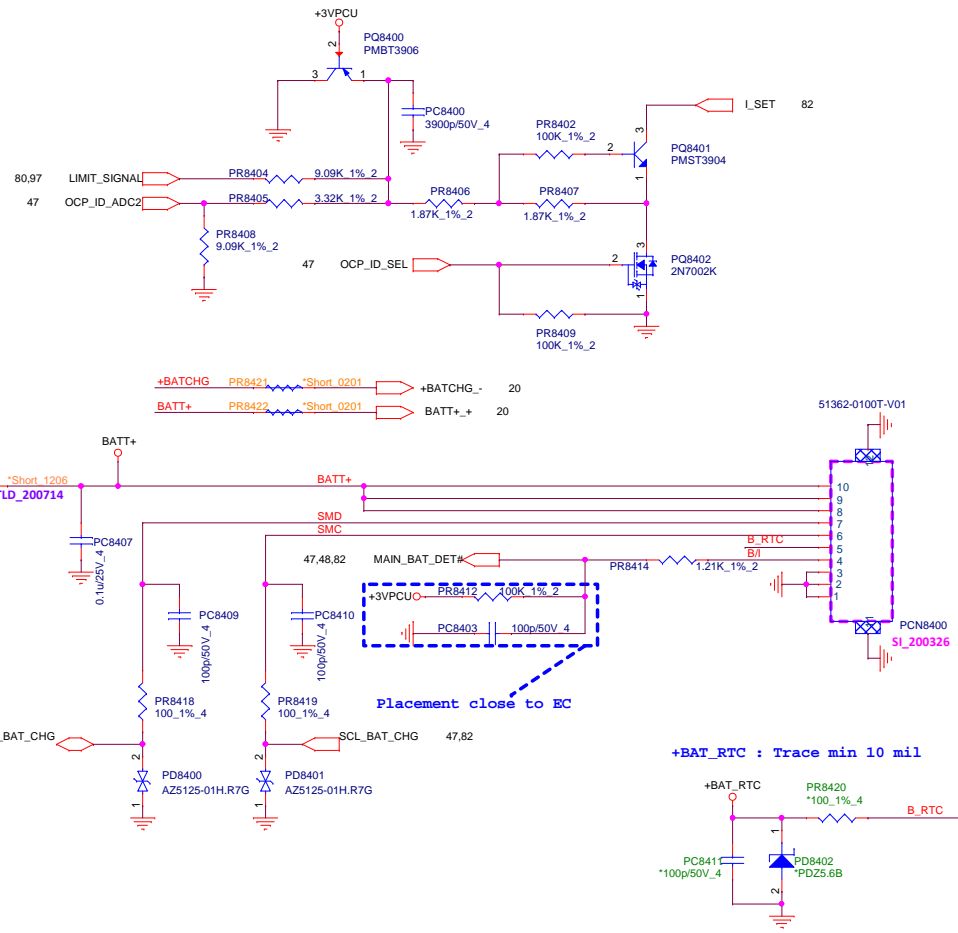



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Quanta X8QA

Size Custom	Document Number 83 -- Charger (ISL9538HRTZ-T)	Rev 1A
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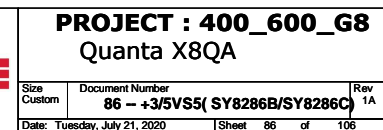
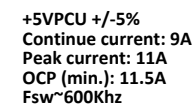
Barrel Adapter OCP

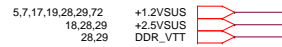


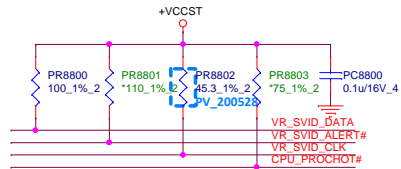


PROJECT : 400_600_G8
Quanta X8QA

Size Custom	Document Number 85 -- Charger II	Rev 1A
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PROG1=63.4Kohm
VBOOT=0V
DVID SR=50mV/us
Decay SR=5000mV/us

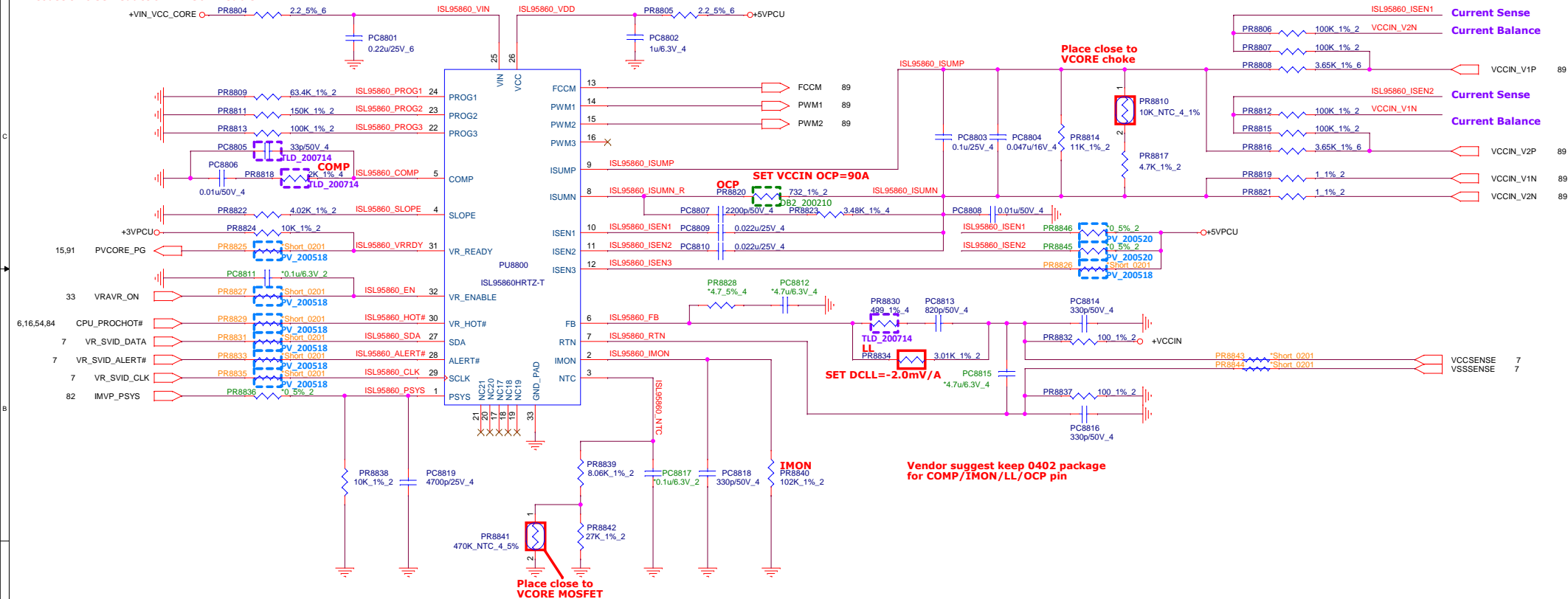
PROG2=150Kohm
IccMax =70A for 2 phase
PS1 Phase Reduction= 1 phase

PROG3=100Kohm
Fsw=750kHz
Acoustic noise Reduction in PS0=Disable

IMVP9 Design: TGL UP3 4+2 (15W)_Performance line
2-phase, Inductor DCR Sensing

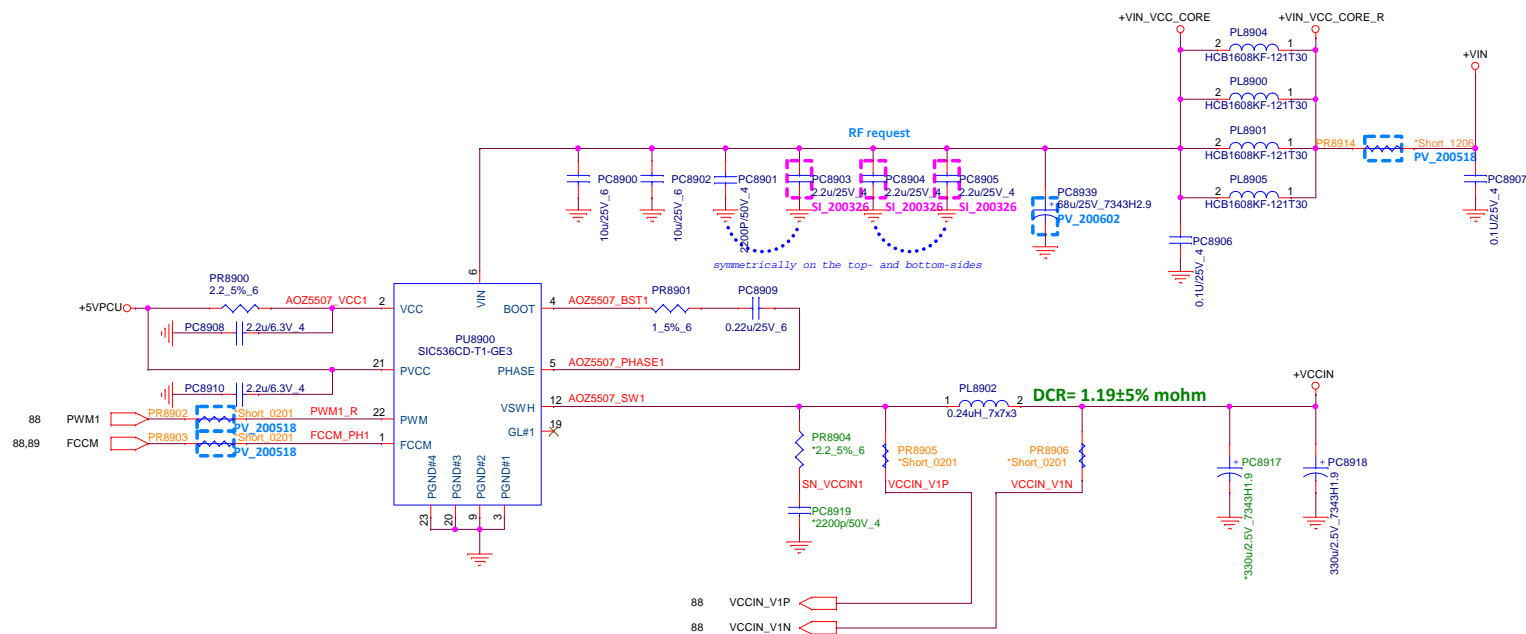
Ref DOC#: 607872 & 575683

VCCIN rail
TDC=36A
Iccmax=55A
Iccmax Transient=65A (10ms)
OCP(min)=90A
DCLL= 2.0mohm
ACLL= 4.4mohm



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Quanta X8QA

Size Custom	Document Number 88 - CPU CORE VR (MP2949A)	Rev 1A
Date: Tuesday, July 21, 2020	Sheet 88 of 106	



IMVP9 Design: TGL UP3 4+2 (15W)_Performance line
2-phase, Inductor DCR Sensing

Ref DOC#: 607872 & 575683

VCCIN rail
TDC=36A
Iccmax=55A
Iccmax Transient=65A (10ms)
OCP(min)=97A
DCLL= 2.0mohm
ACLL= 4.4mohm

Renesas recommended quantity

22u/6.3V_6 x10pcs
330u/2V_7343H1.9 x1pcs
Total 550u

CPU side install

22u/6.3V_6 x9pcs

10u/6.3V_6 x25pcs

Total 448u

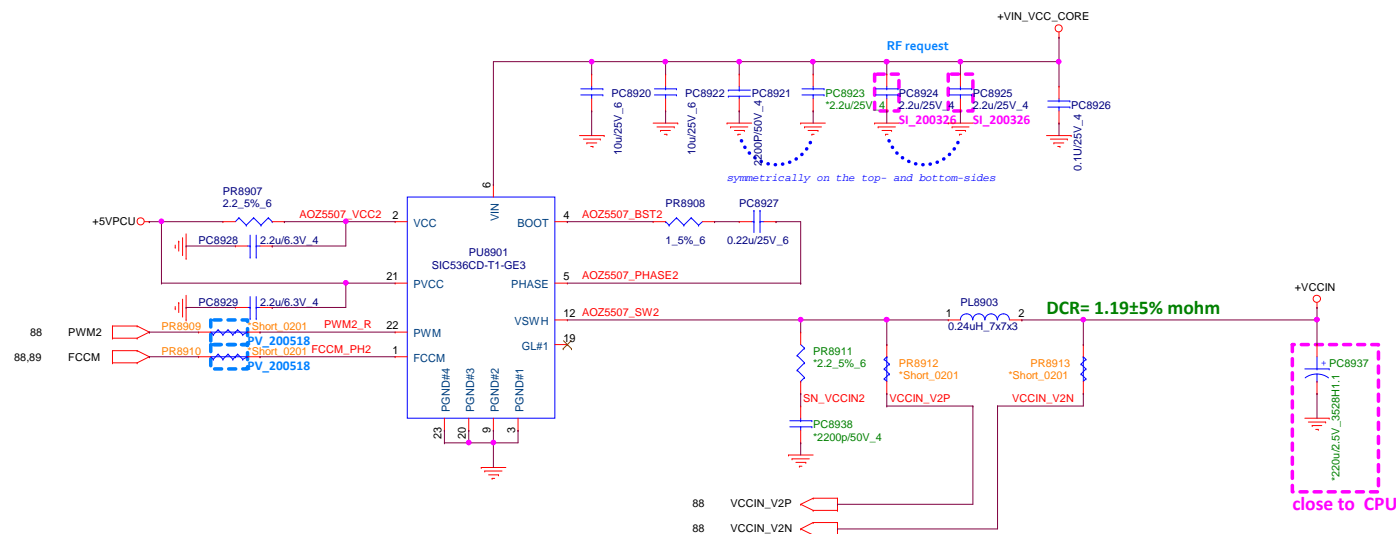
Power side install

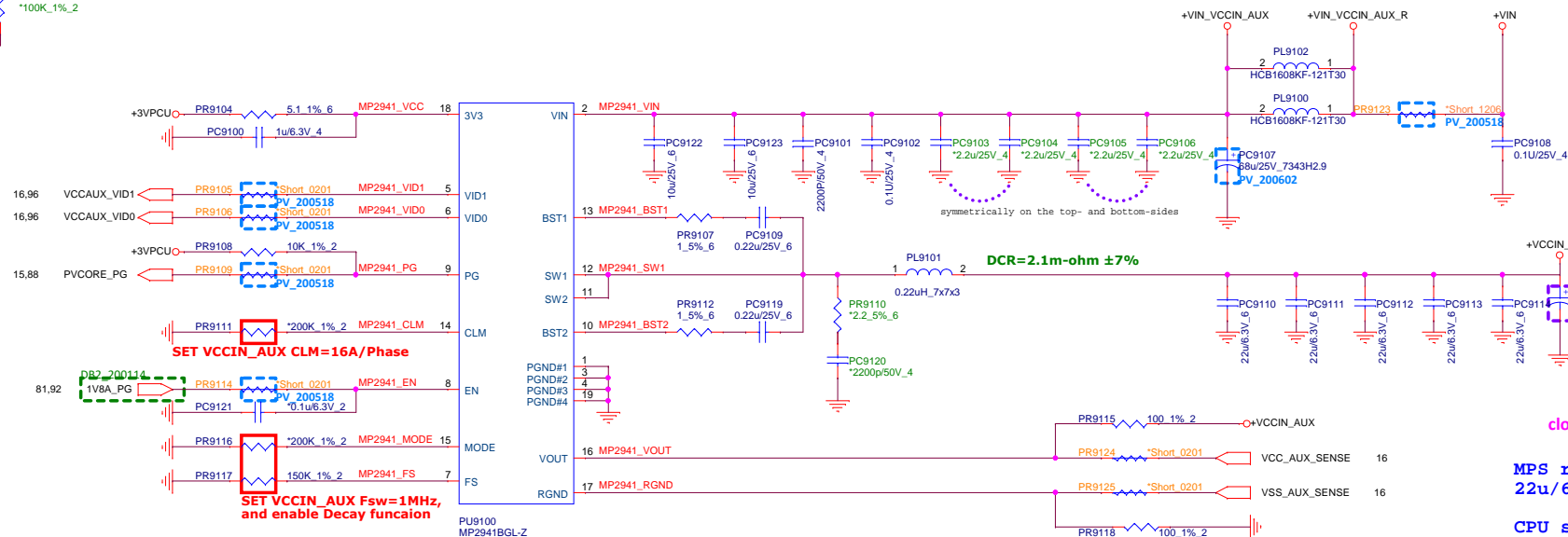
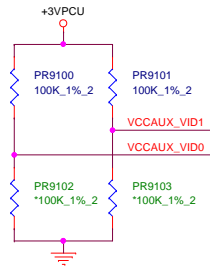
330u/2V_7343H1.9 x1pcs

Total 330u

EE+Power = 748u

Total install can meet Renesas require



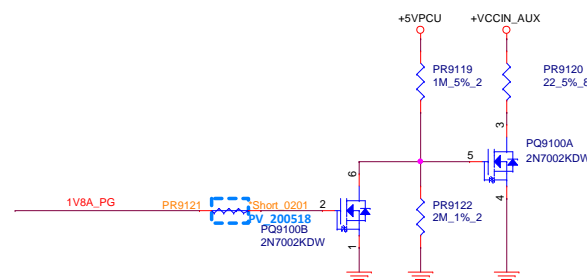


VCCIN_AUX rail
TDC=14A
Iccmax=27A
Iccmax Transient= ???A
DCLL= 0mohm
VBOOT=1.8V

close to CPU

MPS recommended quantity
22u/6.3V_6 x10pcs

CPU side install
22u/6.3V_6 x12pcs
10u/6.3V_6 x25pcs
47u/6.3V_6 x4pcs
Total 702u
Power side install
22u/6.3V_6 x5pcs
Total 110u
EE+Power = 812u



Tabel---1:MODE Select

State	Interleaving	VID Down option	Resistor to GND
M1	N	Slew down	0
M2	Y	Slew down	90k
M3	Y	Decay	150k
M4	N	Decay	>230k or float

Tabel---2:FS Select

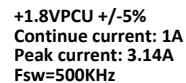
State	Fs (kHz)	Resistor to GND
M1	500	0
M2	700	90k
M3	1000	150k
M4	1200	>230k or float

Tabel---3:CLM Select


State	CLM	Resistor to GND
M1	7A	0
M2	10A	90k
M3	13A	150k
M4	16A	>230k or float

Tabel---4:VID control Bit logics

VID1	VID0	VOUT (V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

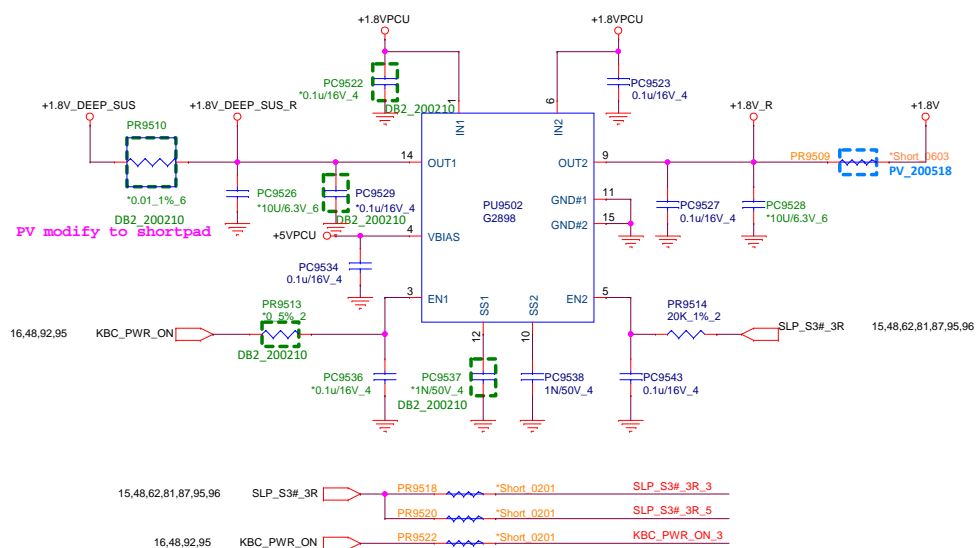
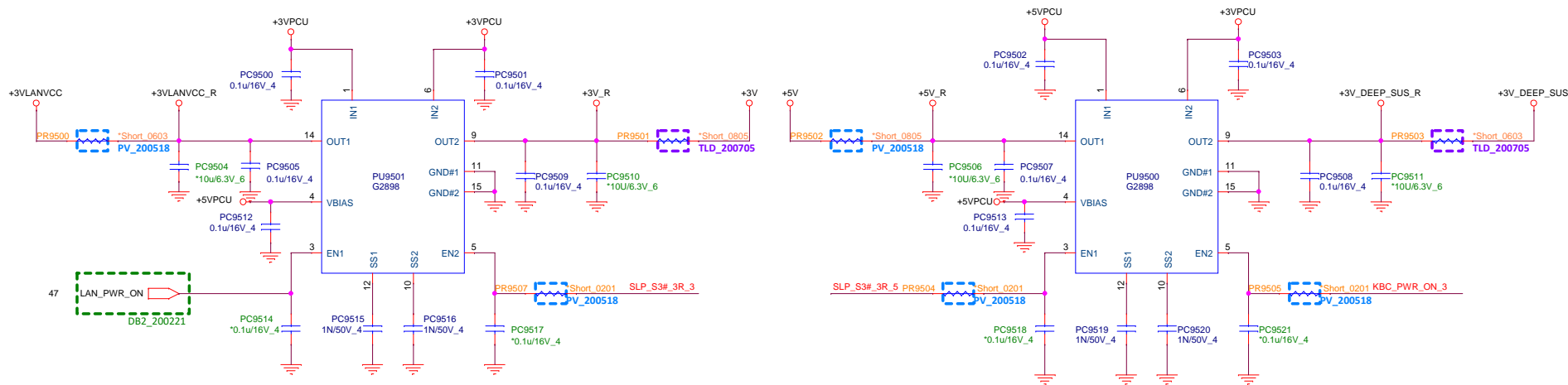


Note: LP#, CO and C1 are pulled high internally



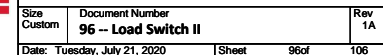
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Quanta X8QA

Size Custom	Document Number 93 -- +1.8VPCU (NB681A)	Rev 1A
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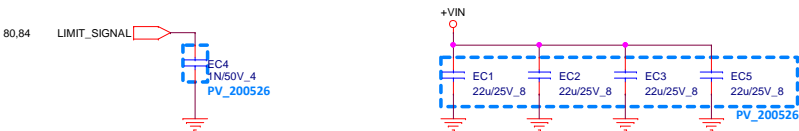


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 8,10,15,16,18,19,33,34,36,41,42,44,47,48,50,52,54,56,58,61,66,72,75,76,77,80,81,82,84,86,87,88,91,92,96,105
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 18,76

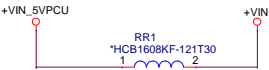
+3V
 +5V
 +3VPCU
 +5VPCU
 +3VLANVCC

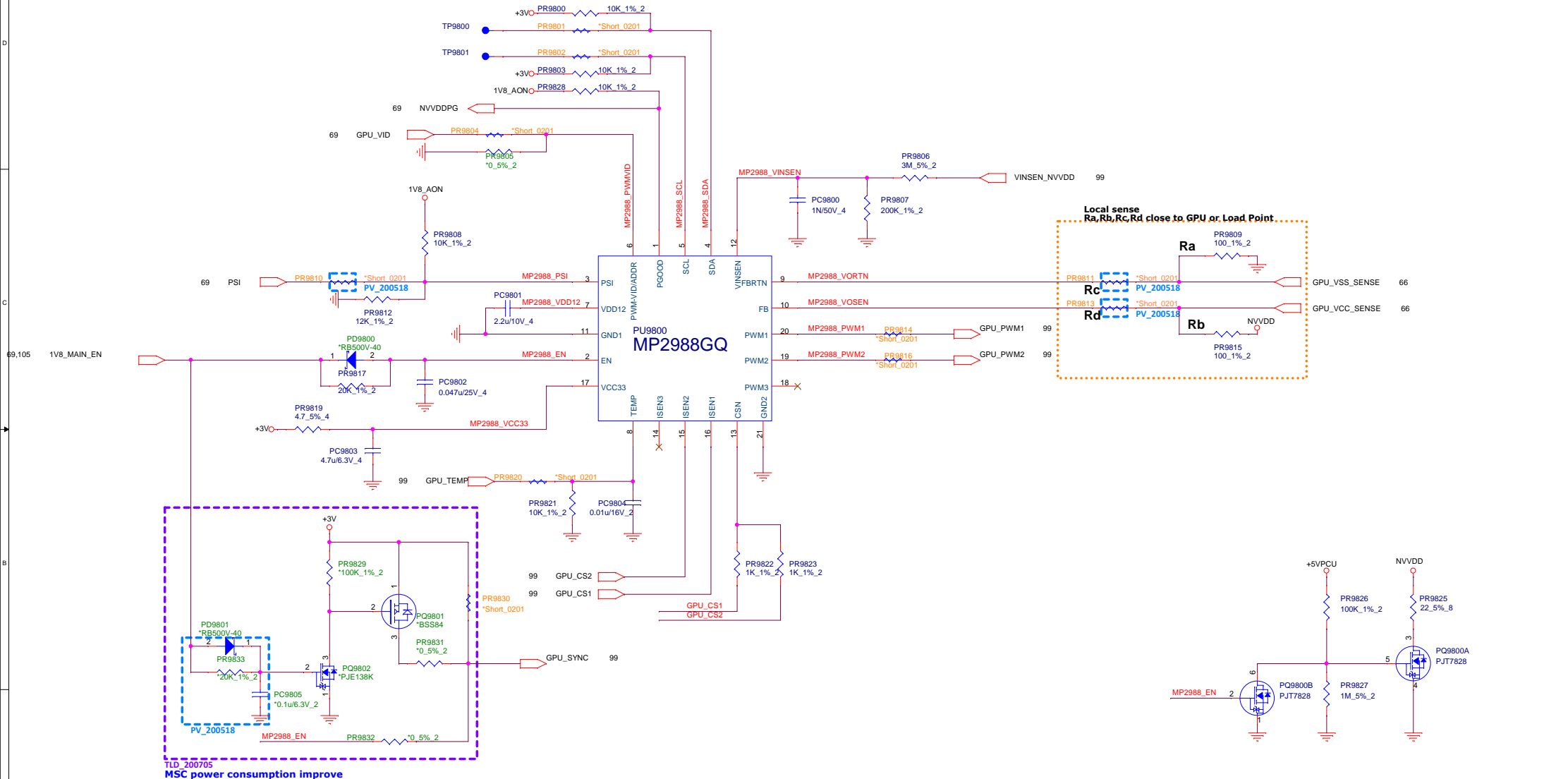


Reserve for EMI & ISEN test



RF Cap

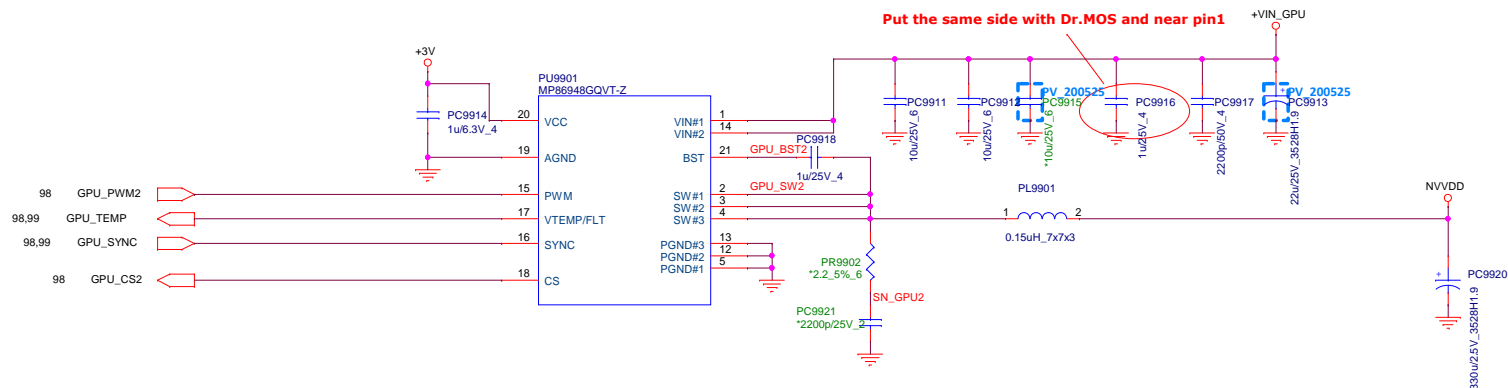
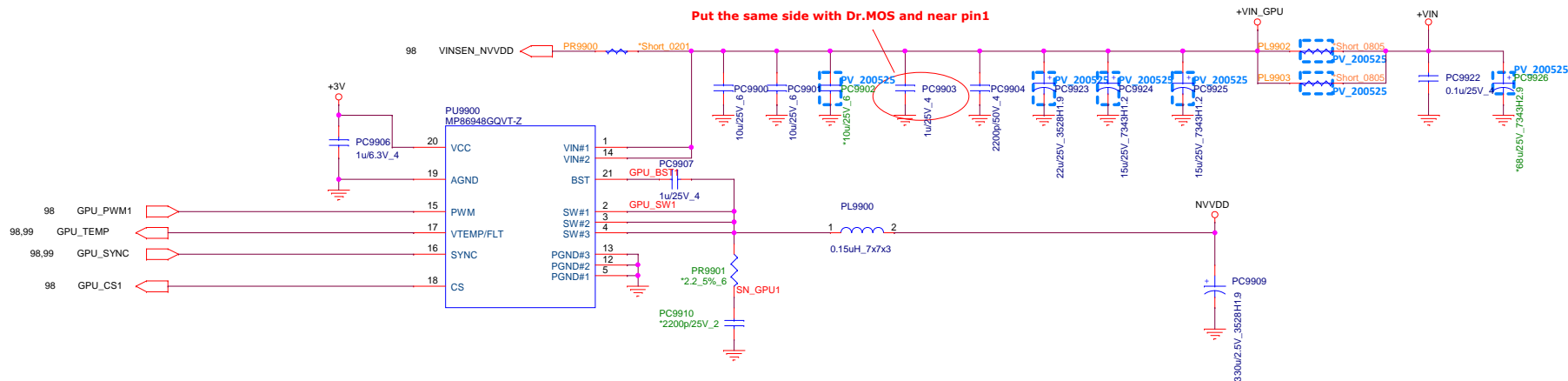


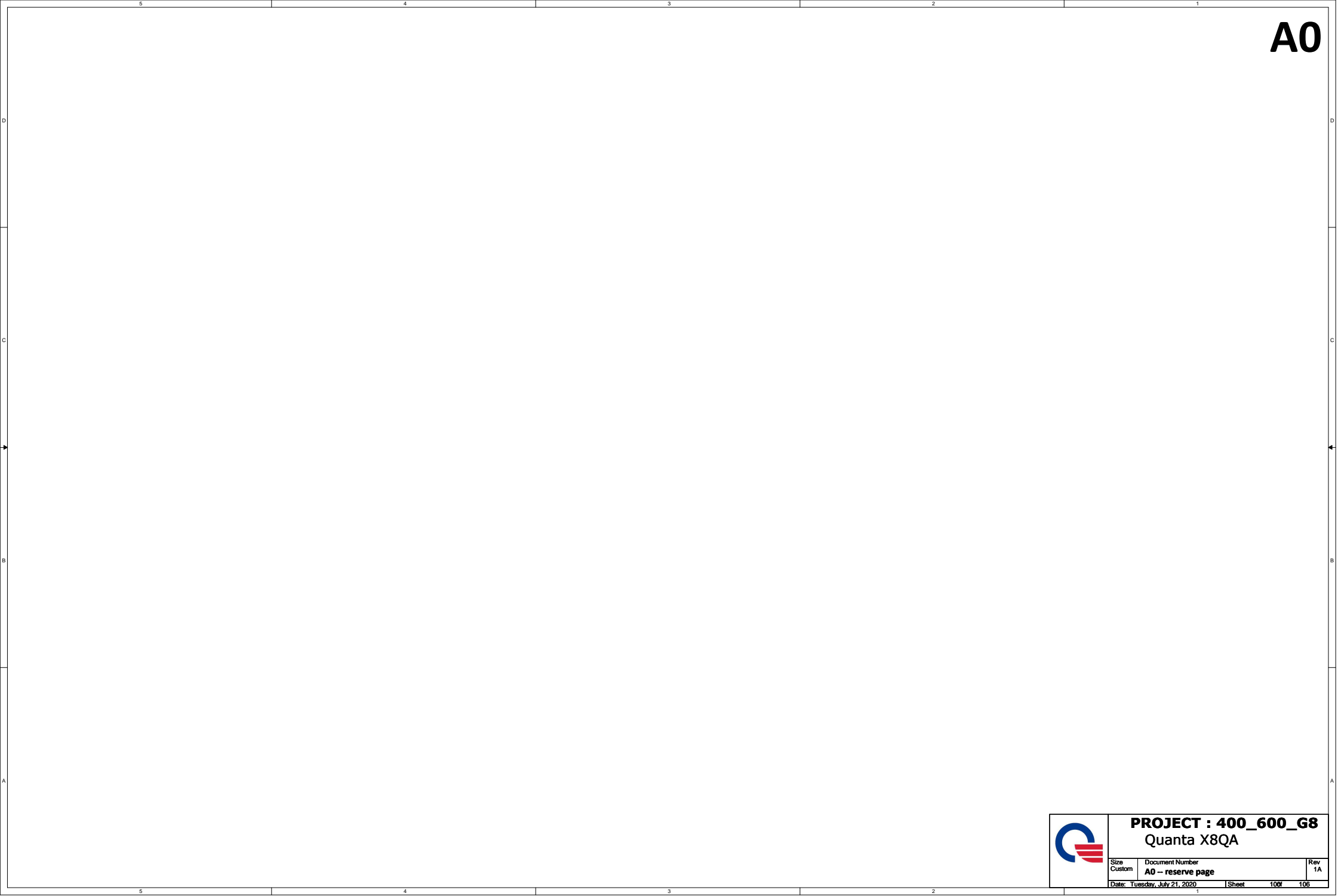



- +VIN_VGACORE
- +3V5
- 1V8_AON
- NVVDD
- +3VPCU

66,67,68,69,105
66,68,99
8,10,15,16,18,19,33,34,36,41,42,44,47,48,50,52,54,56,58

		PROJECT : 400_600_G8 Quanta X8QA	
		7,8,9,10,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42,43,44,45,46,47,48,49,50,51,52,53,54,55,56,57,58,59,60,61,62,63,64,65,66,67,68,69,70,71,72,73,74,75,76,77,78,79,80,81,82,83,84,85,86,87,88,89,90,91,92,93,94,95,96,97,98,99,100	
Size Custom	Document Number +VGACORE (MP2884AGU)	Date: Tuesday, July 21, 2020	Rev 1A

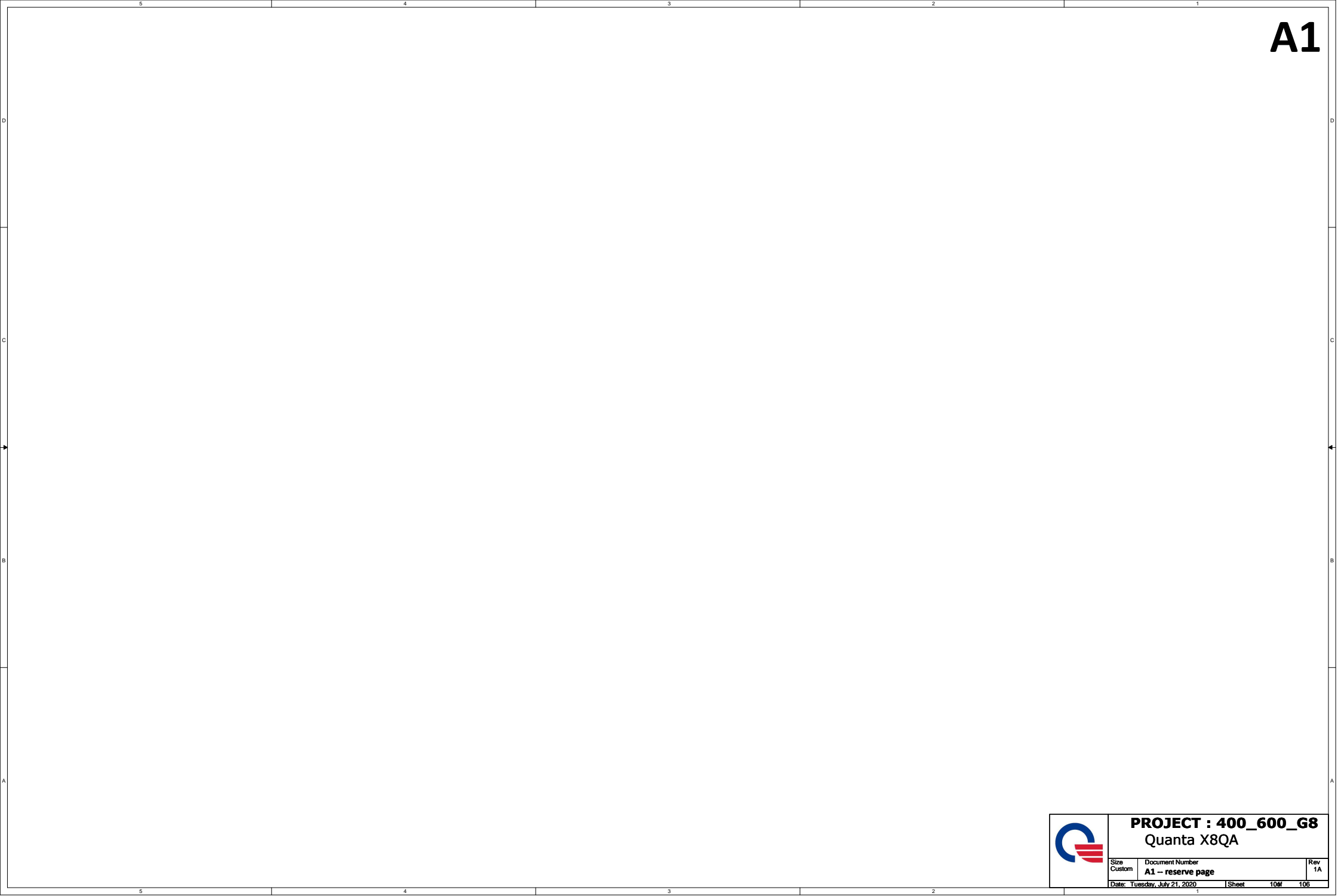







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Quanta X8QA

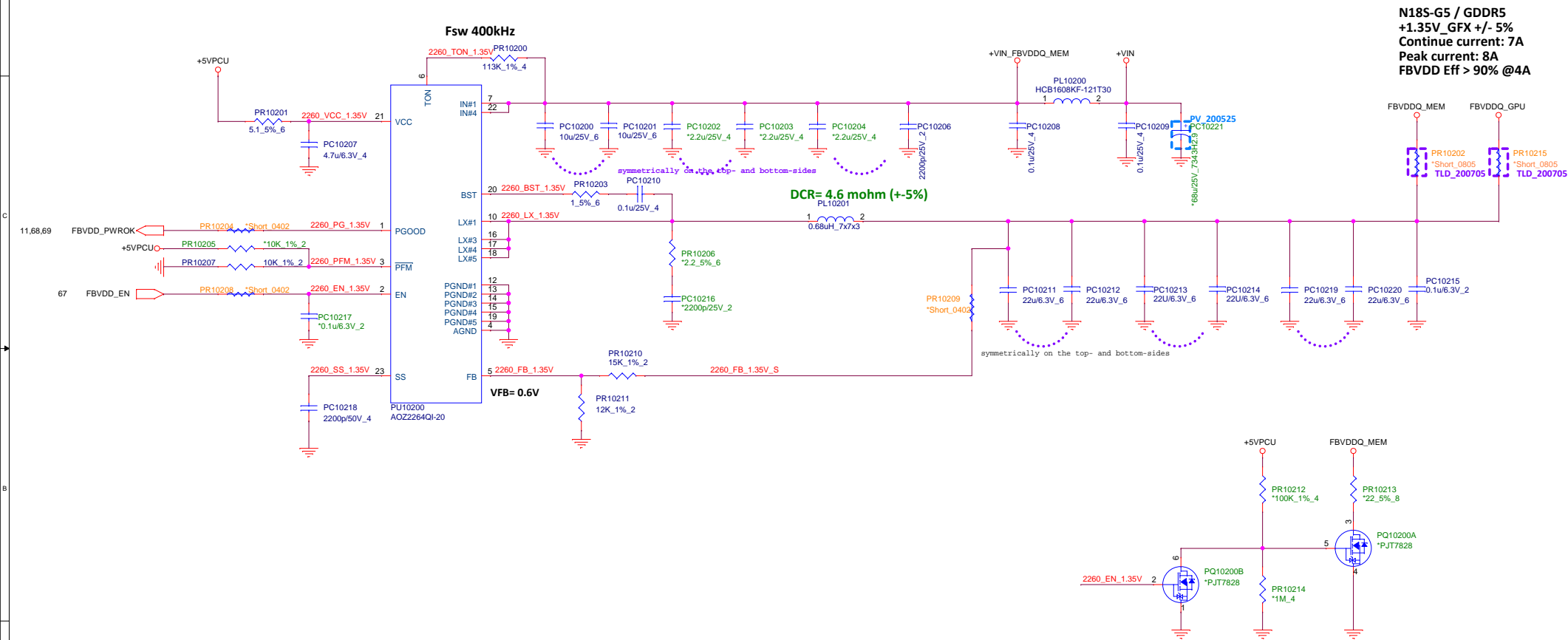
Size Custom	Document Number A0 -- reserve page	Rev 1A
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A3

D

C

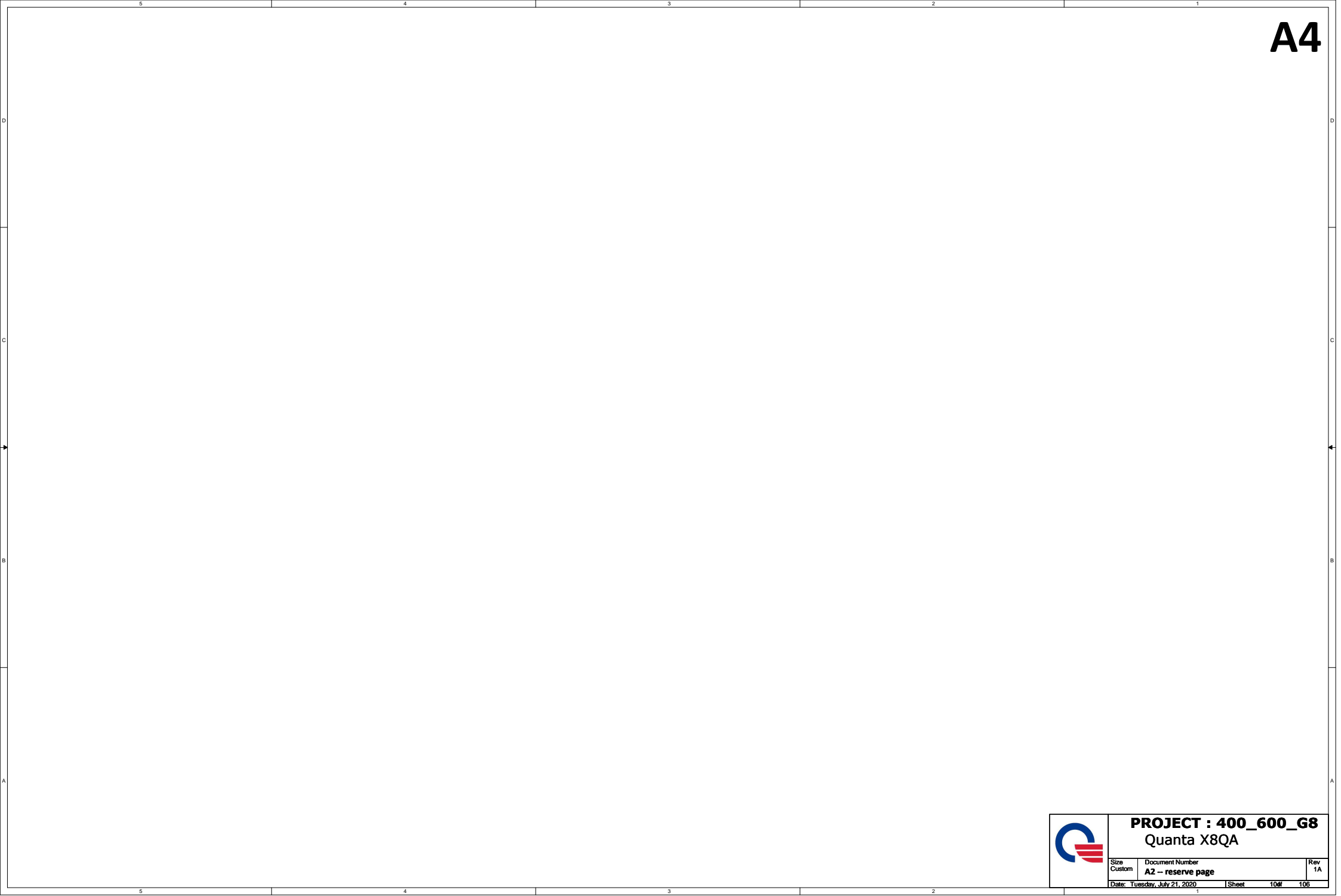
3


A



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Size Custom	Document Number A3 – reserve page	Rev 1A
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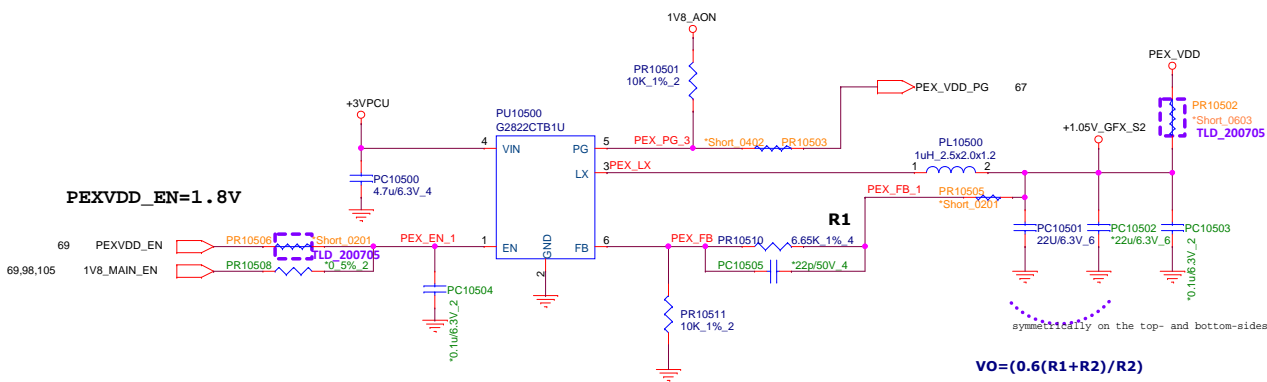


PROJECT : 400_600_G8

Quanta X8QA

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PEXVDD_EN=1.8V



N18S G5
1.0V_PEX +/-5%
Continue current: 1.2A
Peak current: 1.9A
OCP (min.): 3.2A

